Performance Analysis of Novel 600V Super-Junction Power LDMOS Transistors with Embedded P-Type Round Pillars

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***Abstract* — A novel 600V super-junction (SJ) power LDMOS device with two different designs of SJ structures has been proposed. The basic SJ structure consists of a number of p-type round pillars buried in an n-type drift layer down to a p-type substrate. Performance characteristics of the device in terms of the trade-off between on-state resistance and breakdown voltage and the sensitivity of the voltage blocking to charge imbalance in the SJ structure were analyzed by means of 3D numerical simulation. The studies show that designing the SJ structure such that it counteracts the substrate-aided depletion effect leads to a significantly reduced sensitivity of the blocking voltage to charge fluctuation at the expense of a slightly degraded performance trade-off.**

I. INTRODUCTION

The recent realization of the *super-junction* (SJ) concept [1,2] represents a significant breakthrough in overcoming the operation limits of conventional silicon-based high power MOS devices. The SJ concept is based on the principle of charge compensation in alternatively stacked, heavily doped p- and n-type columns, known as *SJ structure*. In the on-state, the heavily doped n-type columns conduct the forward current through the drift zone with strongly reduced on-resistance. In the blocking state, already at a relatively small reverse-biased voltage all the columns are completely depleted of mobile charges. On condition that the space charges in the depleted columns compensate each other, the electric field will be nearly uniformly distributed over the whole drift region. As a result, a substantial increase in breakdown voltage can be achieved.

So far the SJ concept has been commercially realized in vertical double diffused MOS (VDMOS) transistors such as the CoolMOS^{TM} [1] and the MDmesh^{TM} [2]. In lateral double diffused MOS (LDMOS) devices [3,4], however, the presence of the p-type substrate considerably affects the charge compensation in the SJ structure because, under reverse bias, a non-uniform vertical depletion layer forms at the p-substrate/n-drift junction. The normally flat surface electric field becomes distorted by this substrate-aided depletion effect, with the result that the blocking capability of the device deteriorates.

This work deals with the 3D numerical analysis of a novel 600V SJ power LDMOS transistor suitable for use in smart power ICs. Two different SJ structures are considered: one is designed to suppress the substrate effect, whereas the other one serves as reference for comparison. We performed comparative 3D-simulations in order to investigate the performance limitations of the two designs, together with the sensitivity of their blocking capability to the unavoidable doping fluctuations in the SJ structure.

II. DEVICE STRUCTURE

The unit cell of the SJ device is adopted from a RESURF (Reduced Surface Field) LDMOS structure. It has a cell pitch of 10 μm and a length of 50 μm, as depicted in Fig. 1. Its SJ structure comprises five p-type round pillars embedded, at an equal distance to one another, in the n-type drift epilayer of 15 μm thickness down to the very thick, lightly doped p-type substrate.

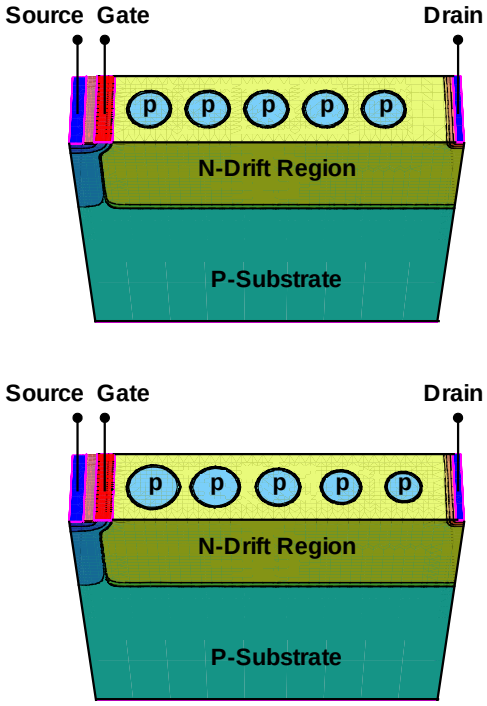


Figure 1: Device structure of the SJ LDMOS under investigation.
Top: uniform SJ. Bottom: non-uniform SJ.

One design, where all the round pillars have the same diameter of 6 µm, is referred to as *uniform SJ*. Although such a uniform structure helps to equally distribute the surface electric field over the drift region, it is not able to efficiently suppress the substrate-aided depletion effect. For this purpose, another structural design, denoted as *non-uniform SJ*, is proposed. Here, the round pillars are arrayed with decreasing size along the entire length of the drift region, starting with the thickest one, whose diameter is 7 µm, near the source and diminishing in steps of 0.5 µm such that the pillar nearest to the drain is thinnest with a diameter of 5 µm. This non-uniform configuration is supposed to counterbalance the gradient in space charge in the substrate during the blocking state.

III. PERFORMANCE TRADE-OFF

It is an inherent feature of power semiconductor devices with high blocking capability that they exhibit substantial power losses in the on-state. There is a trade-off between the specific on-resistance $sR_{DS(on)}$ and the breakdown voltage $V_{BR(DSS)}$. In the theoretical case of an optimum compromise, the two parameters for a RESURF LDMOS device are related by an expression termed *silicon limit* [5]:

$$sR_{DS(on)} = 3.9 \times 10^{3} \cdot A^{1/3} \cdot V_{BR(DSS)}^{7/3} \quad [\Omega \cdot cm^2],$$

where $A = 1.8 \times 10^{-35}$ cm^6 V^{-7} is Fulop's ionization coefficient.

A concurrent variation of the doping levels in the n-drift region and the p-pillars yields the trade-off curves for the two cell layouts, as displayed in Fig. 2 along with the silicon limit line. The drift layer thickness is kept constant at 15 µm. Evidently, the trade-off curve of the uniform design variant lies closer to the silicon limit than that of the non-uniform counterpart. But at high voltage the curve of the non-uniform structure comes closer to the limit line.

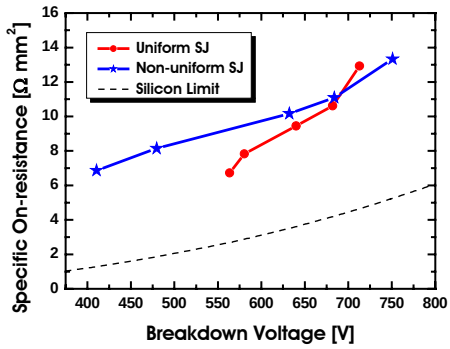


Figure 2: Trade-off between $sR_{DS(on)}$ and $V_{BR(DSS)}$ for two different design variants.

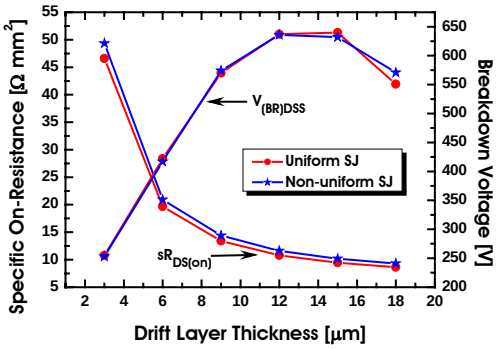


Figure 3: Dependence of $V_{BR(DSS)}$ and $sR_{DS(on)}$ on the epilayer thickness.

Obviously, there is a cross-over point where the two design variants show the same trade-off performance. Of course, the on-state resistance can be reduced by thickening the drift epilayer, i.e. the height of the round pillars, as illustrated in Fig. 3. However, once the layer thickness exceeds a critical value of around 15 µm, premature surface breakdown leads to a significant degradation of the blocking capability.

IV. VOLTAGE BLOCKING SENSITIVITY

Due to unavoidable fluctuations in the fabrication processes one has to accept a certain variation of the doping levels in the the p-type pillars and the n-drift region around the optimum value. The resulting relative deviation, in percent, from the respective optimum doping concentrations is called *charge imbalance* [6].

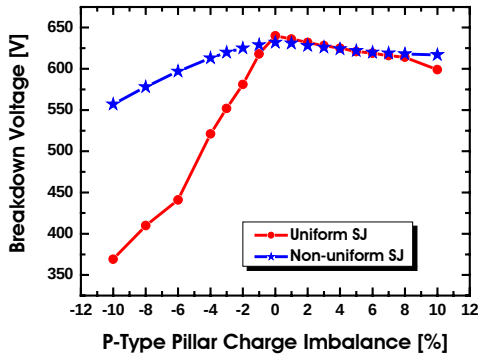


Figure 4: Sensitivity of $V_{BR(DSS)}$ to charge imbalance in the p-type pillars.

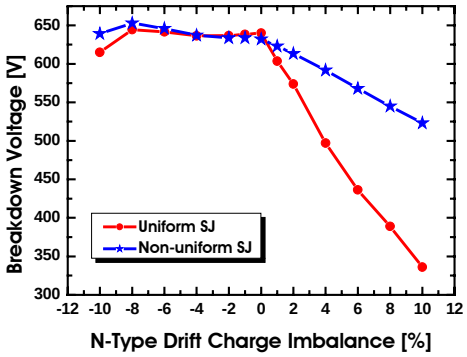
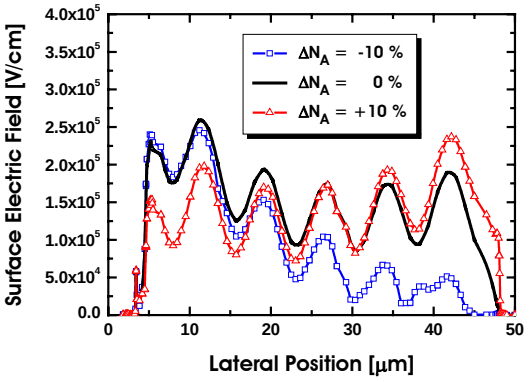


Figure 5: Sensitivity of $V_{BR(DSS)}$ to charge imbalance in the n-drift layer.

Fig. 4 and Fig. 5 show the ability of the two SJ structures to sustain reverse-biased voltage under charge imbalance conditions. Obviously, a deficit of the required optimum doping concentration in the pillars leads to a much more drastic reduction of the breakdown voltage than in the case where the pillars are excessively doped. The opposite effect occurs for the case of charge imbalance in the n-drift layer with the exception that a charge deficiency up to 8% can raise the breakdown voltage to some degree. In any case, the blocking capability of the uniform SJ structure is more sensitive to charge fluctuations than that of the non-uniform one.

Since the p-substrate/n-drift junction near the drain end breaks down at a higher voltage than in the other parts of the device, the dependence of the breakdown



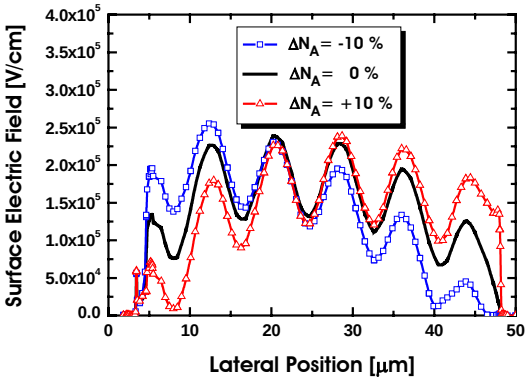


Figure 6: Variation of surface electric field along the cut line through the center of the device with charge imbalance in the p-type pillars.
Top: uniform SJ. Bottom: non-uniform SJ.

voltage on charge imbalance can be related to the displacement of impact ionization from the substrate interface near the drain end towards either the p-base/n-drift or the p-pillar/n-drift junction. For instance, an excessively high doping level in the pillars (Fig. 6) prevents the electric field at the p-base/n-drift junction as well as at the p-substrate/n-drift junction near the drain from reaching the critical value. The resulting surface field profile then increases from the source towards the drain to such an extent that breakdown occurs on the drain side. In contrast, if the space charge in the pillars becomes deficient, the surface electric field will pile up at the source side, thereby shifting breakdown to the p-base region.

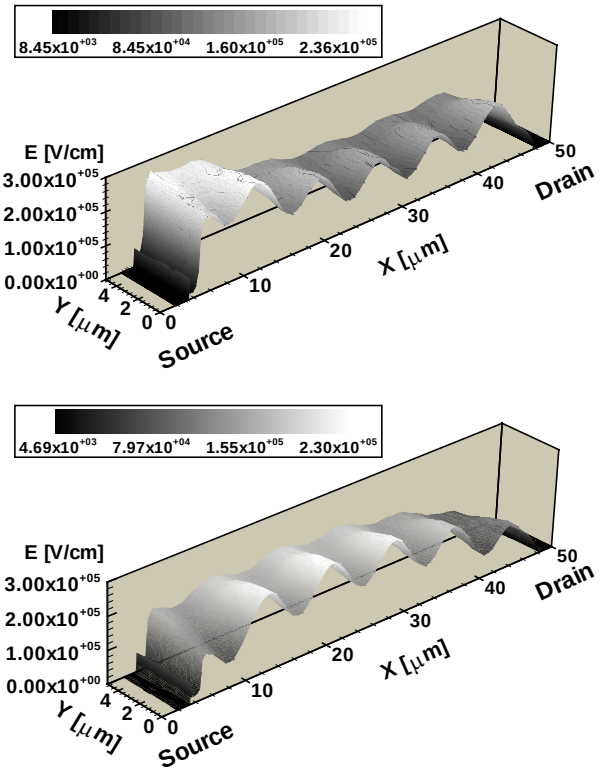


Figure 7: Surface electric field distribution of the device at the maximum breakdown voltage.
Top: uniform SJ. Bottom: non-uniform SJ.

Due to the fact that the maximum electric field is higher at the p-base/n-drift junction than at the p-pillar/n-drift junction, surface breakdown occurs on the source side at lower breakdown voltage than it does on the drain side. This unequal breakdown conditions are responsible for the asymmetric behaviour of the sensitivity curves. At the maximum breakdown voltage the surface electric field distributions of both the uniform SJ and non-uniform SJ have a rather balanced and flat shape except for a periodic ripple which reflects the underlying doping profile. However, the slightly asymmetric surface field profile of the uniform SJ (Fig. 7 top) is more prone to the observed asymmetric breakdown effect than the nearly symmetric profile of the non-uniform SJ (Fig. 7 bottom), which seems to compensate the influence of the substrate-aided depletion. For this reason, an obvious expectation is that a power LDMOS device with non-uniform SJ structure will better sustain dynamic avalanche under unclamped inductive switching.

V. CONCLUSION

We performed a 3D numerical analysis of a novel 600V SJ LDMOS transistor with two different SJ structures in order to evaluate its performance limitations. The simulation results reveal that the device with uniform SJ design has a fairly better trade-off between on-state resistance and breakdown voltage; however, the breakdown voltage of the non-uniform SJ device is much less influenced by charge imbalance in the SJ structure.

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