Statistics of Grain Boundaries in gate poly-Si

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***Abstract*- A nanometer-scale variation due to grain boundaries in gate poly-Si is investigated in detail assuming arrangement of grain boundaries obeys the Poisson distribution. Statistics of grain boundaries described here enables us to understand nanoscopic fluctuation in leakage current and threshold voltage shift in MOSFETs. For the first time, these nanoscopic fluctuation and arrangement variation of grain boundaries are related.**

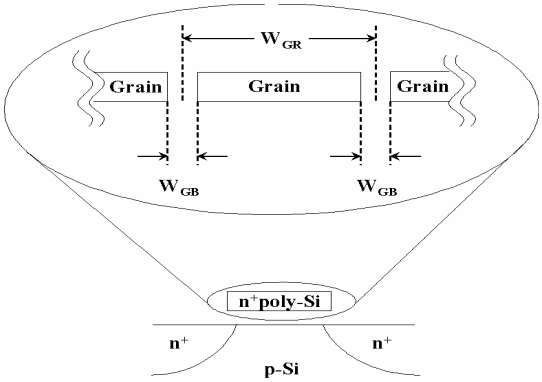

Figure 1: Cross-sectional view defining grain boundaries.

I. Introduction

Aggressive scaling of MOSFETs is increasing effects of grain boundaries in gate poly-Si on transistor performance. A nanometer-scale variation in arrangement of grain boundaries is investigated in detail assuming the Poisson distribution for this nanoscopic variation. As a result, we explain a relation between peaks shown in frequency distribution of gate leakage current and the arrangement of grain boundaries. It is also found that the nanoscopic variation of this arrangement causes fluctuation of threshold voltage (V_T), since drain-to-gate leakage current (DGLC) is affected by grain boundaries.

II. Origin of fluctuations in gate current

Impurities in poly-Si trend to concentrate on near grain boundaries [1]. Since higher concentration in poly-Si increases direct tunneling, gate current concentration may be higher near the grain boundaries. If a grain boundary locates on near the Source-Drain edge (SDE) region in which electron flux concentrates in the substrate, then gate current may become further higher. The gate current may therefore depend on arrangement of grain boundaries.

III. Statistics of Grain Boundaries

Firstly, in order to study statistics of grain boundary we quantify fluctuation in gate current. Fig. 1 is a cross-sectional view of nMOSFET including grain boundaries whose widths of grain and grain boundary are W_{GR} and W_{GB}, respectively. Assuming that W_{GB} is a constant, there can be m (=L_G/W_{GB}) sites which n grain boundaries can occupy, as shown in Fig. 2. Here we assume W_{GB} is 3nm and the SDE overlap (Yj) is 4.5nm.

We denote increase of gate current by Δ_j (j=1, 2… m) when there is a grain boundary in the j-th site. Fig. 3 shows the calculated Δ_j is larger in SDE region than in channel region, which is due to concentration of current flux.

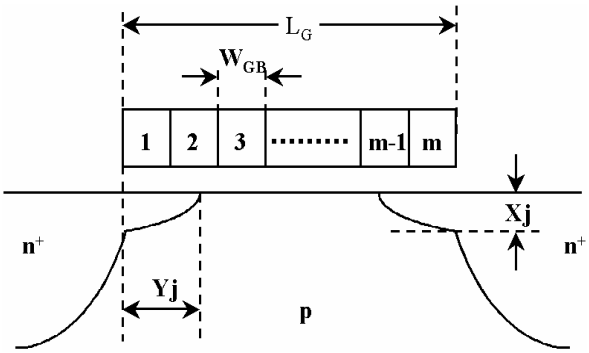

Figure 2: Cross-sectional view of nMOSFET with grain boundaries, which is used in the present simulation. The first and m-th sites belong to the SDE region.

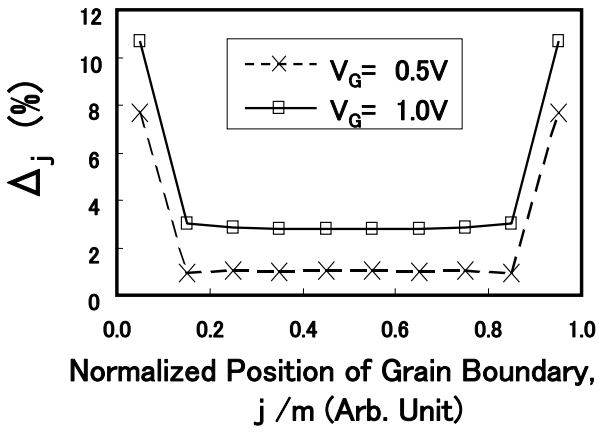

Figure 3: Position dependence of Δj which is a component of a fluctuation vector when j=1, 2…10 and L_G=30nm and T_{OX}=1.3nm.

The present simulation using the method published in [2, 3] successfully obtains good agreements with measurements of gate currents, as shown in Fig. 4.

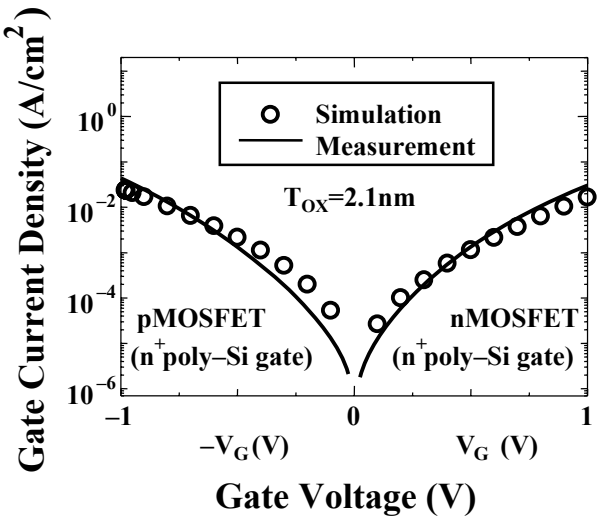

Figure 4: Measured and simulated J_G-V_G curves.

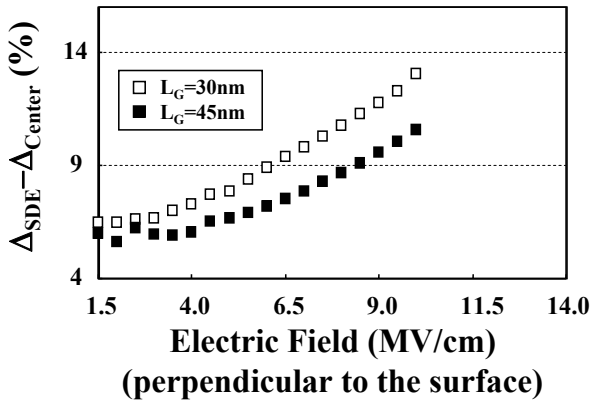

Figure 5: Electric field dependence of Δj. Since Yj is fixed, Δ_j in smaller L_G is more enhanced by grain boundary at the SDE region.

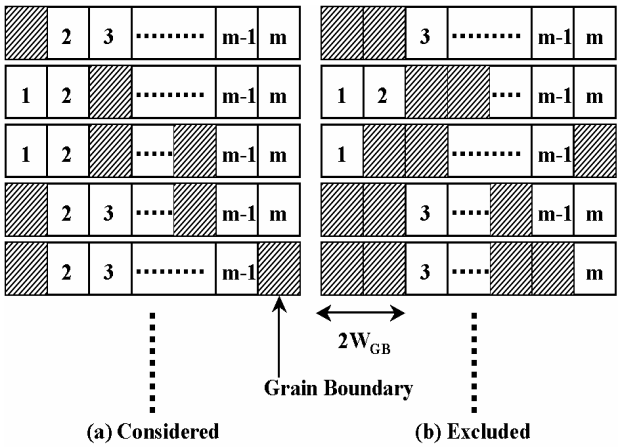

Figure 6: Arrangements of grain boundaries in the gate. We take into account arrangement states described in (a) and exclude arrangement states described in (b). The reason that the grain boundaries are assumed to locate separately among the sites is that two grain boundaries occupying nearest-neighbor sites are regarded as a grain boundary with a width of $2W_{GB}$, as seen in (b).

A difference between Δ_j in SDE and channel regions increases with an averaged vertical electric field and with the decrease f the gate length (L_G), as shown in Fig. 5. This means that position dependence of Δ_j becomes more notable with the scaling of MOSFETs.

Considering all the arrangements in which any two sites are separate for W_{GB} not to be doubled, as shown in Fig. 6, we obtain frequency distribution of gate current shown in Fig. 7 (a). There appears a confusing structure with a lot of peaks there. Next, describing an average of W_{GR} by $\langle W_{GR} \rangle$, the Poisson distribution is written by $P_n (L_G, \langle W_{GR} \rangle) = (L_G/\langle W_{GR} \rangle)^n \exp(-L_G / \langle W_{GR} \rangle)/n!$, giving a probability that we have n grain boundaries in the gate whose length is L_G. We subsequently define g (m, n) as the number of cases in which n grain boundaries are arranged among m sites, excluding cases in which nearest-neighbor sites are

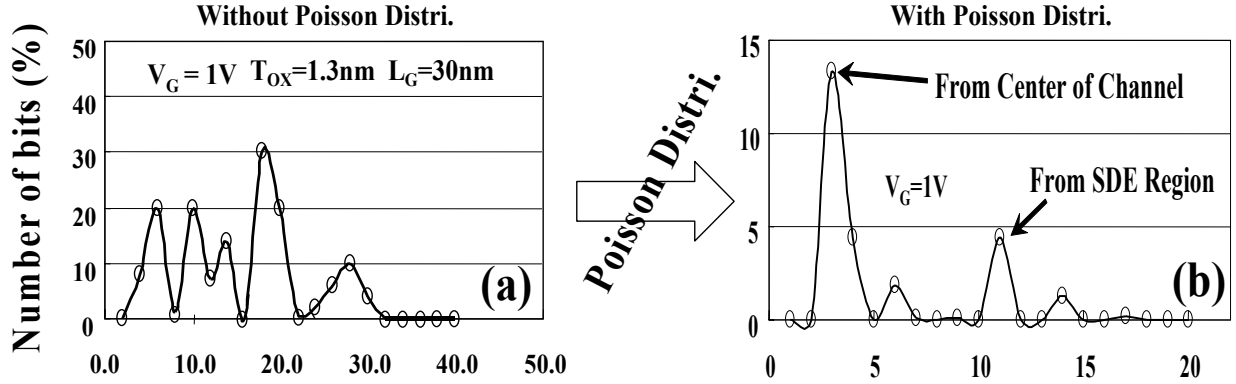

Figure 7: Frequency distribution with regard to increase of gate current per bit that is obtained by ($\theta_{m,n}$,Δ).

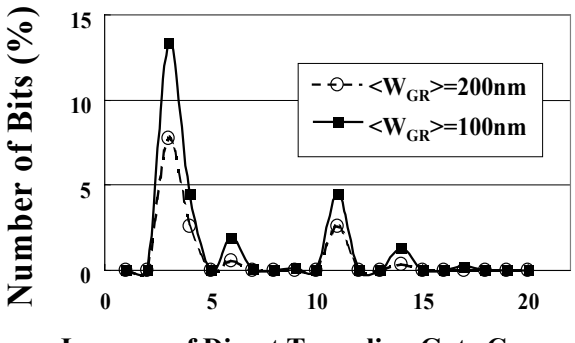

Figure 8: $<W_{GR}>$-dependence of the frequency distribution when L_G=30nm, T_{OX}=1.3nm, and V_G=1.0V.

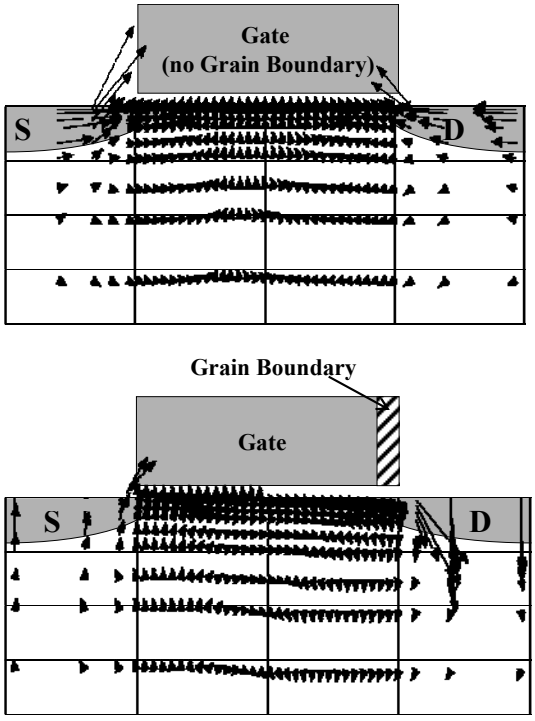

Figure 9: Electron current flow distribution in the substrate with or without a grain boundary at the drain edge. The DGLC occurs at the drain edge due to the grain boundary, as shown in the right. The arrows in the gate have been omitted to make the figures transparent.

occupied by two grain boundaries. If we set a site with a grain boundary to '1' and another site with no grain boundary to '0', then we can write the arrangement of grain boundaries by a vector, $\theta_{m,n}$, for example, $\theta_{m,n}$ = (…,0,1,0,0,1,…). We can also define a vector, $\Delta = (\Delta_1,\Delta_2,\ldots,\Delta_m)$. Here a scalar product, $(\theta_{m,n}, \Delta)$, denotes an increase of direct tunneling with regard to the arrangement $\theta_{m,n}$. Let us consider the case of m=3. If n = 0, then we have g (3, 0) =1 and $\theta_{3,0}$ = (0, 0, 0), resulting in the increase of the direct tunneling being obtained by $(\theta_{3,0}, \Delta) = 0\cdot\Delta_1 + 0\cdot\Delta_2 + 0\cdot\Delta_3 = 0$. If n=1, then we have g (3, 1) =3 and $\theta_{3,1}$ = (1, 0, 0), (0, 1, 0), and (0, 0, 1), resulting in the increase of the direct tunneling being Δ_1, Δ_2, Δ_3, respectively. If n=2, then we have g (3, 2) =1 and $\theta_{3,2}$ = (1, 0, 1), resulting in the increase of the direct tunneling being $\Delta_1+\Delta_3$. The number of bits associated with $(\theta_{m,n}, \Delta)$ is calculated by multiplying the number of bits and P_n (L_G, $<W_{GR}>$) / g (m, n). We can thus regulate frequency distribution of gate current increase, as shown in Fig. 7(b). This analysis requires less number of data $(\Delta_1,\Delta_2,\ldots,\Delta_m)$ to deduce the frequency distribution, which substantially reduces computational time.

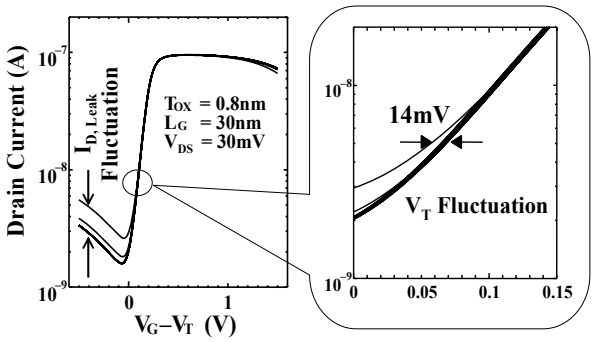

Figure 10: Variation of V_T

IV. Results

The confused structure shown in Fig. 7 (a) is turned out to be a transparent structure of peaks shown in Fig. 7 (b) taking into account the Poisson distribution. When V_G=1V, there are four peaks at Δ=3%, 6%, 11%, and 14%. The 3% and 11% peaks come from grain boundaries in the channel region and in the SDE region, respectively, as shown in Fig. 3. The 6% peak is composed of two grain boundaries in the channel region since Δ=6%=3%+3%. The 14 % peak is composed of the first grain boundary in the SDE region and the second grain boundary in the channel region since Δ=14%=11%+3%. Fig. 8 shows that these peaks become lower as $<W_{GR}>$ increases, which means that fabrication process for polygate should be optimized to enlarge $<W_{GR}>$. Fig. 9 shows that DGLC occurs due to a grain boundary at the drain edge side. Consequently, fluctuation of grain boundaries causes fluctuations of V_T with $\Delta V_T \leq 14$mV and of drain leak ($I_{D,\,Leak}$) with $\Delta I_{D,\,Leak}$ being a few nA, as shown in Fig. 10. The fluctuations of $\Delta V_T > 0$, $\Delta V_T \cong$ −a few mV, and $\Delta V_T \cong -10$mV attribute to grain boundaries between center of channel and SDE, near center of channel, and at the drain edge, respectively, as shown in Fig. 11(Left). The fluctuation of $\Delta I_{D,\,Leak}$ is also shown in Fig. 11(Right). A relation between $\Delta I_{D,\,Leak}$ and ΔV_T is shown in Fig. 12. It is found that points of dominant contribution deduced by the Poisson

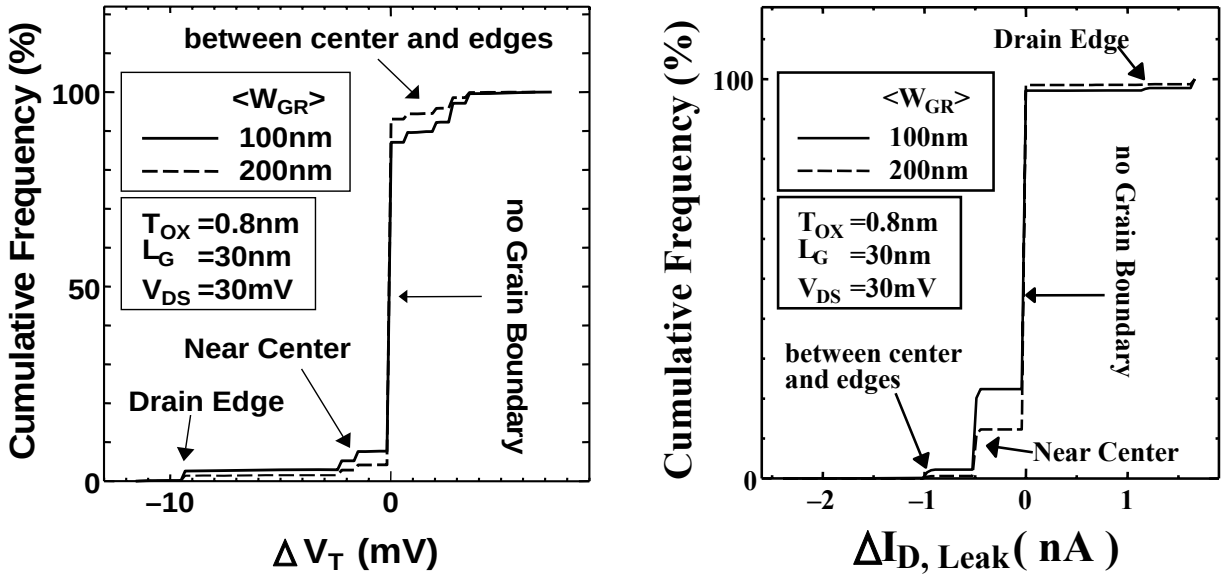

Figure 11: Cumulative frequency of $\Delta I_{D,\,Leak}$ and ΔV_T that are defined as difference measured from "no grain boundary". Fluctuations in both $\Delta I_{D,\,Leak}$ and ΔV_T are enhanced as $<W_{GR}>$ is decreased. This is consistent with Fig. 8.

distribution are close to a straight line, while points of less contribution are apart from the line.

V. Conclusions

It is shown that the arrangement vectors and the Poisson distribution analysis of grain boundaries deduces clear frequency distribution of gate leakage current. We relate the peaks in the frequency distribution to nanoscopic variation in arrangement of grain boundaries, and show that DGLC modulated by grain boundaries causes a few nA fluctuation in $I_{D,\,Leak}$ and a few ten mV fluctuation in V_T for L_G=30nm even if there is no fluctuation of impurities. This grain boundaries fluctuation is therefore essential to V_T of narrow gate width device such as SRAM. The scaling of MOSFET enlarges fluctuations of both V_T and $I_{D,\,Leak}$ since the SDE overlap become larger compared to L_G and higher electric field enlarges Δ_j, as shown in Fig. 5. A way to suppress these fluctuations is to optimize fabrication process to increase $<W_{GR}>$, as shown in Figs. 8 and 11. The analysis based on the Poisson distribution reveals a linear relation between $\Delta I_{D,\,Leak}$ and ΔV_T, as shown in Fig. 12.

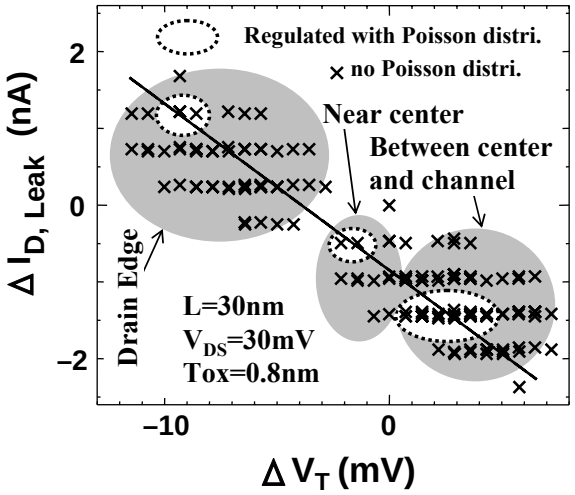

Figure 12: Relation between I_{OFF} and V_T.
The crosses correspond to the arrangement vector ($\theta_{m,n}$) and depict data before regulated by the Poisson distribution. The dotted circles depict data of dominant contribution deduced by the Poisson distribution.

References

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[2] H. Watanabe and S. Takagi, "Effect of incomplete ionization of impurities in poly-Si gate and band gap narrowing on direct tunneling gate leakage current", J. Appl. Phys. **90**, pp.1600-1607 (2001)

[3] H. Watanabe, K. Matsuzawa, and S. Takagi, "Scaling effects on gate leakage current", Trans. ED. **50**, pp. 1779-1784 (2003).