Intrinsic parameter fluctuations in MOSFETs due to structural non-uniformity of high-κ gate stack materials

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***Abstract* – Non-uniformity of the dielectric properties of high-κ material due to random grain orientation and phase separation will lead to variation in characteristics between different devices. Here we present a model for phase separated high-κ dielectrics and investigate, by means of 3D numerical device simulation, the intrinsic parameter fluctuations which result from this structural non-uniformity.**

I. INTRODUCTION

As the scaling of MOSFETs continues, the requirement to maintain electrostatic integrity dictates an aggressive reduction of the oxide thickness below 1 nm, introducing intolerably high gate leakage [1]. This has led to the introduction of high-κ materials in the gate stack, offering the required SiO_2 equivalent oxide thickness at increased physical thickness and reduced gate leakage. There are many technological issues [2] associated with the use of high-κ material in the MOSFET gate stack leading to mobility degradation and instabilities. Some of these factors will also introduce intrinsic parameter fluctuations in the corresponding MOSFETs, similar to the fluctuations introduced by random discrete dopants and oxide thickness variations [3]. In this paper we investigate intrinsic parameter fluctuations in decananometre bulk MOSFETs introduced by non-uniformity of the dielectric properties of the high-κ material due to random grain orientation and phase separation [4]. Such variations in the film structure are illustrated in Figure 1 which shows a plan-view TEM image of a HfSiO film, with phase separation between HfO_2 crystalline regions and the amorphous SiO_2 matrix [5]. The gate stack structure will vary from one device to another, resulting in the fluctuation of parameters between devices. The associated effects of mobility degradation in the devices fabricated with this type of gate dielectric are not considered at this stage.

II. SIMULATION TECHNIQUE

The simulations were carried out with the 3D Glasgow ‘atomistic’ device simulator [6] which is based on the drift-diffusion approximation and employs density gradient quantum corrections. The simulator has been modified to include spatial variations in gate dielectric associated with structural non-uniformity of the high-κ gate stack. To illustrate the effect we have carried out simulations in the case of crystalline phase separation, where grains of high-κ material (e.g. HfO_2) with different crystal orientation interface each other, or are embedded within a SiO_2 matrix.

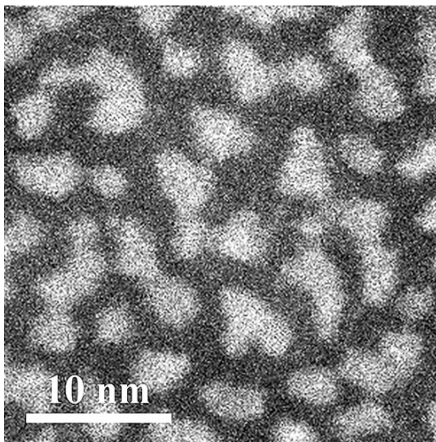

Figure 1: Plan-view TEM image of a HfSiO film [5] illustrating phase separation of the Hf and Si oxides.

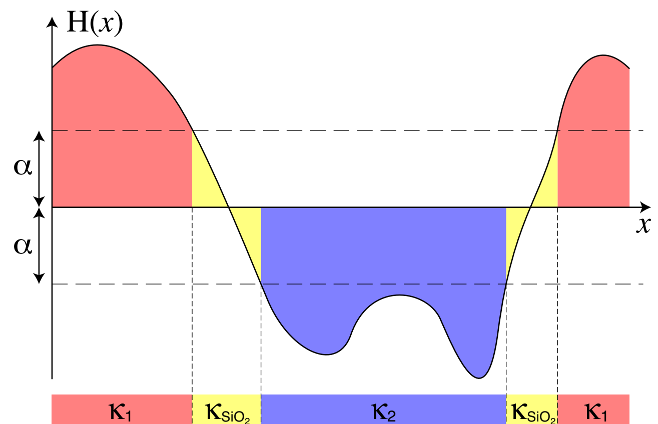

Figure 2: Method used for allocating dielectric properties based on the generation of a random surface.

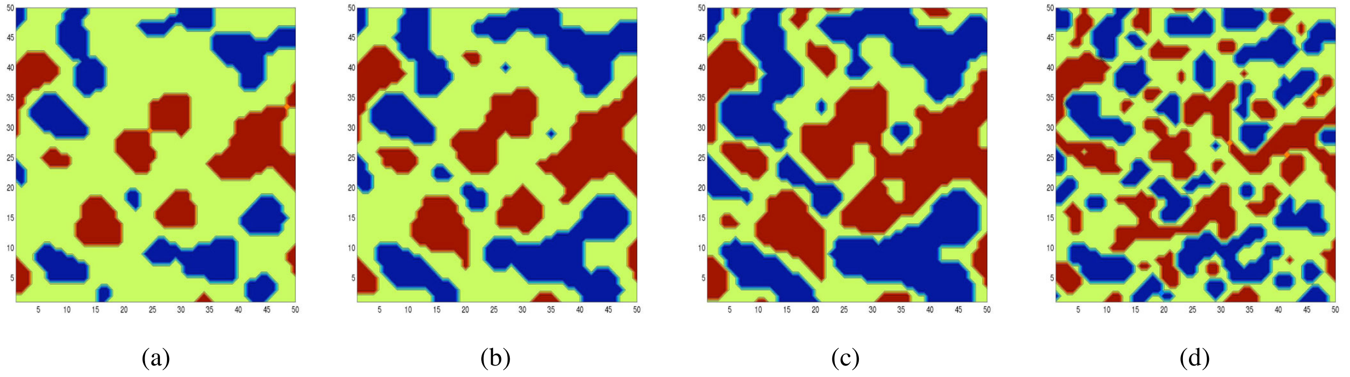

Figure 3: Dielectric patterns produced by the model with different parameters: (a) $\alpha = \Delta$, $\Lambda = 5$ nm, (b) $\alpha = 0.75\Delta$, $\Lambda = 5$ nm, (c) $\alpha = 0.5\Delta$, $\Lambda = 5$ nm, (d) $\alpha = 0.75\Delta$, $\Lambda = 2.5$ nm.

The TEM image of Figure 1 illustrates typical phase separation of HfSiO into HfO_2 poly crystal regions and a SiO_x matrix resulting from high temperature annealing. There is a definite characteristic length to the spacing of the HfO_2 crystals, and the crystal size is on a scale of approximately 5nm. This suggested that a statistical approach for generating the structure of the high-κ dielectric should be adopted. Our approach is based on the 2D Fourier synthesis technique which has been previously utilised for the generation of random surface roughness patterns [3]. A random surface is generated with given statistical parameters, rms amplitude, Δ, and correlation length, Λ. First a complex array with $N \times N$ elements is constructed, whose amplitude is determined by the power spectrum obtained from a Gaussian autocorrelation function with the specified values of Δ and Λ. The phases of the elements are selected randomly, ensuring that each surface is unique. Several conditions [7] must be satisfied to ensure that the corresponding 2-D surface in real space, obtained by inverse Fourier transformation, represents a real function, $H(x,y)$.

Figure 2 shows how this random surface, H, can be used to assign the dielectric constants to the different materials in the gate oxide. A single parameter α, chosen to be a particular fraction of Δ, controls the phase separation with SiO_2 assigned for $-\alpha < H < \alpha$, and high-κ dielectric assigned in the rest of the material. This provides the structure evident from the TEM image (Figure 1) consisting of isolated grains of high-κ material surrounded by SiO_2. Figure 3 shows the effect of varying the parameters α and Λ on the generated

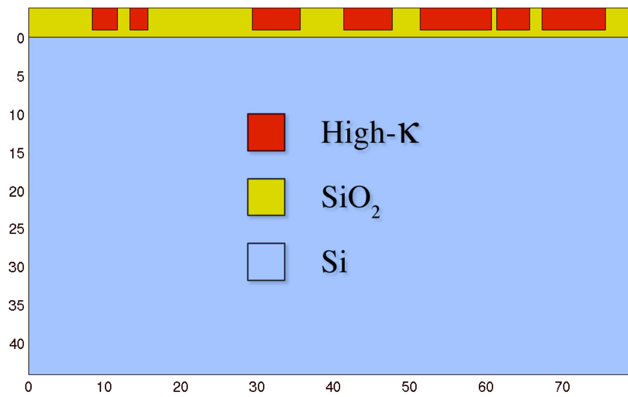

Figure 4: The vertical description of the dielectric properties for an example random pattern. The high-κ grain boundaries are assumed to be vertical and a 0.5 nm SiO_2 interfacial layer is included.

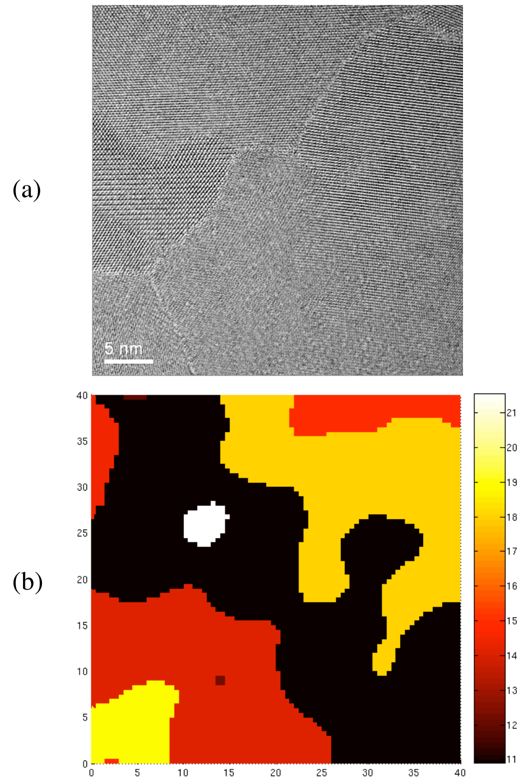

Figure 5: (a) Plan view TEM image showing grains of HfO_2 each with random orientation and (b) an example of a random dielectric pattern generated by the presented model with $\alpha = 0$ (i.e. no SiO_2).

patterns. Reducing the value of α reduces the separation between regions of different high-κ dielectric, and reducing α to zero removes the phase separation. Changing Λ alters the overall scale of the random pattern and is adjusted to give grain sizes of approximately 5 nm. Figure 4 shows the projection of the random pattern vertically within the gate stack. The grain boundaries are assumed to be vertical and an SiO_2 interfacial layer of 0.5 nm is included.

A recursive search algorithm has been implemented to identify connected areas of high-κ which allows individual “grains” to be identified and allocated a random dielectric constant, within a given range, to reflect a random grain orientation. However, for this initial investigation a single value of dielectric constant is used for all high-κ regions.

Even if the phase separation can be avoided in processing the recrystallisation of the high-κ material could result in a poly-crystalline structure with grains, each of which can have a random orientation as is shown in the TEM image of Figure 5(a). By reducing the factor α to zero in the model the phase separation can be removed leaving regions of high-κ each of which can have a random dielectric assigned. However, as it is apparent from Figure 5(b) the presented model does not accurately capture the characteristics of the shape and boundary connectivity of the grains in the TEM image. We therefore restrict this investigation just to the effects of phase separation until a better model for random grain orientation can be developed.

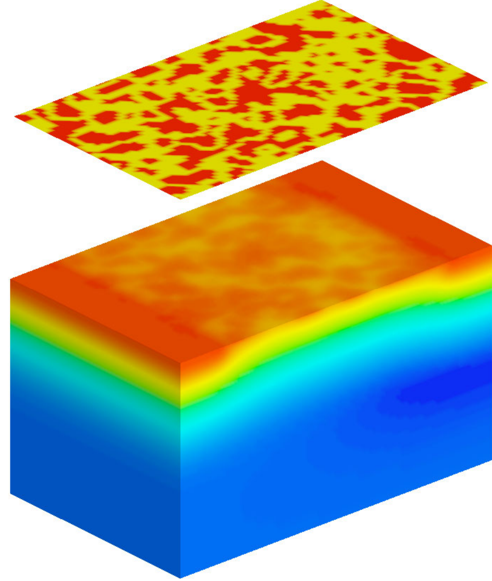

Figure 6: Electrostatic potential in a 50×50 nm MOSFET showing the fluctuations in surface potential due to the spatial variations in gate dielectric. The dielectric pattern is shown in the plane above.

II. SIMULATION RESULTS

The potential drop between gate and channel in the regions of high-κ will be less than across regions of SiO_2. This will lead to spatial fluctuations in the surface potential which will inevitably lead to variations in device characteristics from one device to the next. Figure 6 shows the electrostatic potential within a MOSFET, clearly demonstrating the fluctuations in surface potential due to structural variations in the gate oxide. The random dielectric pattern is shown in the plane above the device with the regions of high-κ dielectric producing higher surface potentials than in those parts of the channel below an SiO_2 region.

I_D-V_G characteristics for ten 50×50 nm MOSFETs with random high-κ patterns are shown in Figure 7 demonstrating the spread in threshold voltages. The parameters used in the phase separation model for these simulations are $\alpha = 0.7\Delta$ and $\Lambda = 3$ nm as these parameters produce patterns on the same scale as the features in the TEM image of Figure 1.

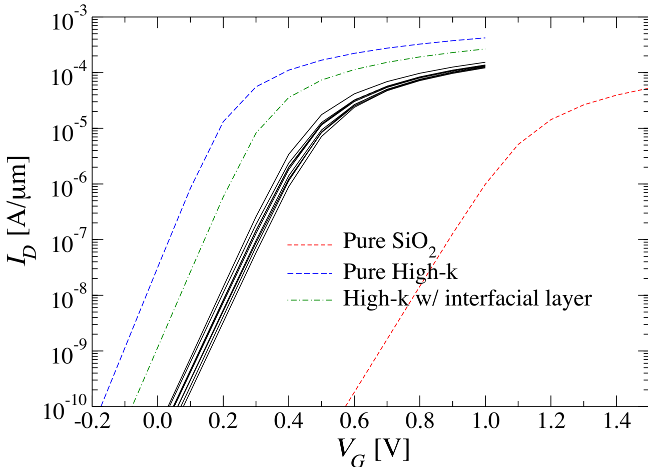

Figure 7: I_D-V_G characteristics for 10 devices with random dielectric pattern, and the limiting cases.

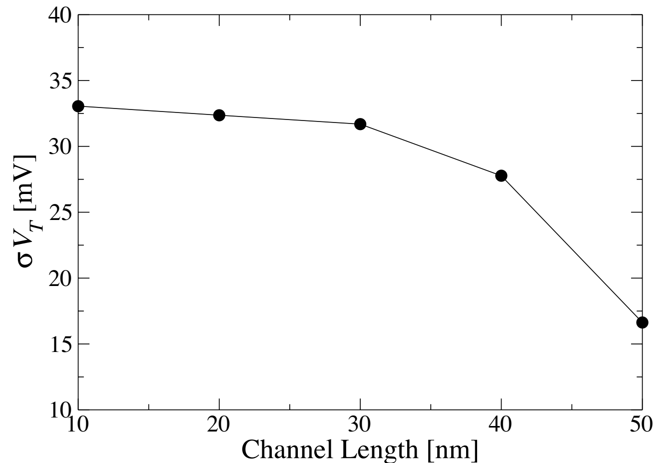

Figure 8: Dependence of σV_T on channel length for samples of 200 devices with random gate dielectric patterns.

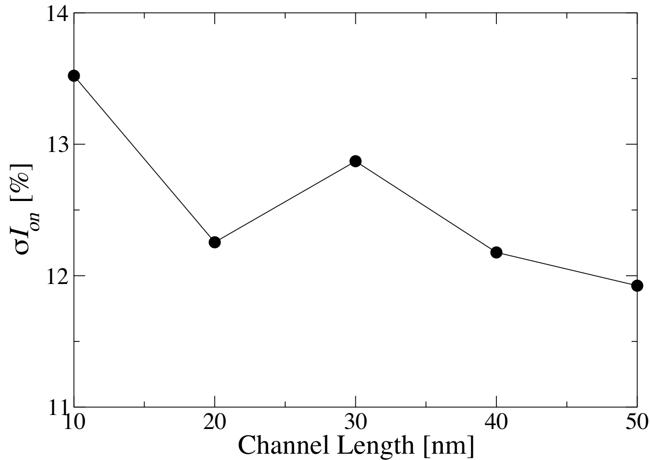

Figure 9: Dependence of σI_{on} on channel length for samples of 200 devices with random gate dielectric patterns.

Here a single value of dielectric constant ($\varepsilon = 20\ \varepsilon_0$) is used in the high-κ regions. Also shown are the curves for a pure SiO_2 gate oxide and pure high-κ (above an interfacial layer). These two conditions will be the limiting cases for the fluctuations and the curves from devices with random phase separation patterns will lie between these two curves. In all cases the gate oxide is 4 nm thick, and the expected degradation in subthreshold slope due to the reduced gate oxide capacitance when SiO_2 is used, is evident.

In Figure 8 the standard deviation in threshold voltage, σV_T, for a sample of 200 devices, each with a different gate dielectric pattern, is shown for different channel lengths. This increases as the channel length is reduced below 50 nm, however it saturates at shorter channel lengths to a value of approximately 33 mV. This saturation behaviour is characteristic of intrinsic parameter fluctuations which are caused by stochastic structural variations which can be modelled using this Fourier synthesis technique. As the device feature size approaches the correlation length of the fluctuations the boundaries imposed by the limiting cases discussed above restrict the magnitude of the fluctuations. This behaviour has also been observed in the cases of oxide thickness variation [3].

Figure 9 shows the dependence of the fluctuations in on-current, σI_{on}, on the channel length. This demonstrates that for the channel lengths and device structure considered here there is very little change in the fluctuations with channel length, with σI_{on} being approximately 12-13% in each case. However in such conditions, in addition to the fluctuations due to variations in the electrostatics within the device, which are fully captured by the drift-diffusion simulator, there will be increased scattering from the potential fluctuations within the channel which will lead to variations in the transport from device to device. The magnitude of this additional contribution to the parameter fluctuations can only be assessed using Monte Carlo simulations which include *ab initio* scattering from the potential fluctuations through the real space trajectories of the carriers. These simulations will be presented at a later stage.

CONCLUSIONS

We have developed a model for the structural non-uniformity in high-κ gate stacks which results from phase separation of composite high-κ gate dielectrics. This is based on the allocation of material parameters based on a random rough surface obtained from a 2D Fourier synthesis where the correlation length, Λ, and the phase separation parameter, α, can be adjusted to match the distributions observed experimentally. We have shown that the spatial variation in dielectric constant throughout the gate stack will lead to parameter fluctuations between devices.

ACKNOWLEDGEMENTS

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