Full Three-Dimensional Analysis of a Non-Volatile Memory Cell

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Abstract

We demonstrate the applicability of three-dimensional process simulation and show its benefit for the development of modern semiconductor technology. Therefore we have performed a process simulation for a Caywood-EEPROM memory cell, followed by the extraction of the coupling capacitance. Such a kind of analysis allows to optimize the layout of the EEPROM memory cell as well as the process parameters. Additionally we show that it is sufficient for the simulation of various process steps to apply simplified empirical models without loosing accuracy in the extracted parameters since the physical behavior of deposition and etching processes is often empirically well characterized within a certain process window.

1 Introduction

Due to the growing complexity of the structures of modern semiconductor devices, especially in the field of non-volatile memories, but also in the field of classical CMOS technology three-dimensional semiconductor process simulation gradually gains more importance. In this work we focus on non-volatile memories (NVM) which play an important role in modern system on chip solutions. The increasing demand of user-programmable information in such systems has led to new challenges in designing systems with a certain amount of integrated memory. Since SRAM and DRAM data is lost when no power supply is present, non-volatile memories are the only possibility to provide flexible applications for mobile and small systems, which require variable information storage. Among the known architectures, the Caywood cell, which has been developed by J.M. Caywood [1], combines good endurance and reliability with a simple structure and good performance with average area consumption. This Caywood cell has been analyzed by means of process simulation to characterize the impact of layout and process modifications.

2 Simulation Environment

For performing the three-dimensional process simulation flow the topography simulator TOPO3D [2] has been used. In order to capture all structural relevant properties within the simulation flow, various models available in TOPO3D have been applied for the

individual process steps. Thereby the computation time can be kept low without losing accuracy.
Common to all models available in TOPO3D is the concept of calculating topography fronts and performing boolean operations with the calculated front (topography front) and the original structure [2]. Worth mentioning is that each process simulation step of TOPO3D is finalized by a volume mesh update which allows to apply finite-element analysis to all intermediate results or to include other volume mesh based process simulation tools into the process flow.

3 Simulation Flow

For the simulation of the Caywood-EEPROM memory cell seven simulation steps had to be performed. The simulation starts with the oxidation of the field oxide. Due to the two-dimensional nature of this problem this simulation step was carried out with DIOS-ISE [3].
By adding the floating gate to the structure, the actual three-dimensional simulation starts. Therefore a layer of polysilicon is deposited by the empirical isotropic deposition model of TOPO3D. This model performs the surface propagation by applying a cellular algorithm [4], and it extracts the final triangulated topography front using advanced smoothing and simplification techniques [5]. A homogenous deposition rate applied to all regions of the surface suffices to describe the physical phenomena and in addition the model demands only low computation time.
The formation of the floating gate itself is performed by the empirical etching model of TOPO3D, which is coupled with an aerial image simulation [6]. The mask information is taken from a gds2-file containing a 3×3 cell array to prevent disturbances because of simulation domain boundaries. On this mask data an aerial image simulation is performed (the result is shown in Figure 1).

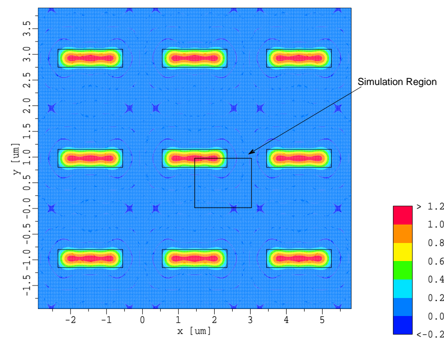

Figure 1: Aerial image simulation result of the fbating gate mask of a 3×3 EEPROM cell array [6]

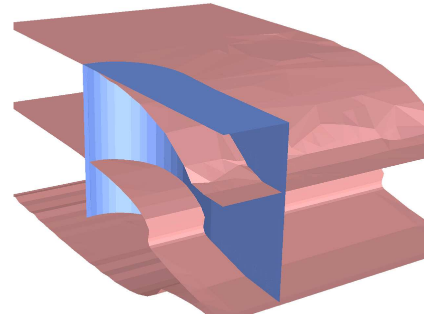

Figure 2: Topography front (blue) resulting from the aerial image mask generated by the empirical etching model and the surface of the input structure (red).

This aerial image is provided as input for the etching model. The generation of the topography front within the model is performed by triangulating the aerial image data and extending the planar structure along an isoline of the aerial image profile into the third

dimension as shown in Figure 2. The isoline threshold was chosen to match a typical characteristic dimension of a long isolated line. All regions of the exposed material in the input structure, which are not covered by the topography front, are removed by the post-processing operation of the etching model. Parts of the topography front, which penetrate untouched regions (eg. visible within the field oxide region in Figure 2), are eliminated in the first phase of the post-processing procedure. This model is very efficient concerning computational resources and delivers sufficiently accurate results as has been shown by comparison with experiments (Figure 3).

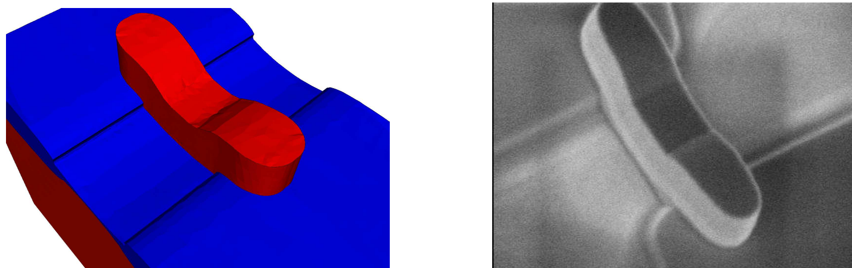

Figure 3: Simulated (left) shape of the fbating gate and SEM picture of the fbating gate (right)

The floating gate formation is followed by an oxidation which is approximated in our simulation approach by a deposition of silicon-dioxide. In order to perform this simulation step the isotropic deposition model is used as well as for the first poly-silicon layer deposition. The major difference between these two deposition steps is the significantly higher cellular resolution for the oxide deposition. The higher resolution is required to accurately resolve the thin oxide layer with the drawback of a significantly higher computation time due to the larger number of surface cells.

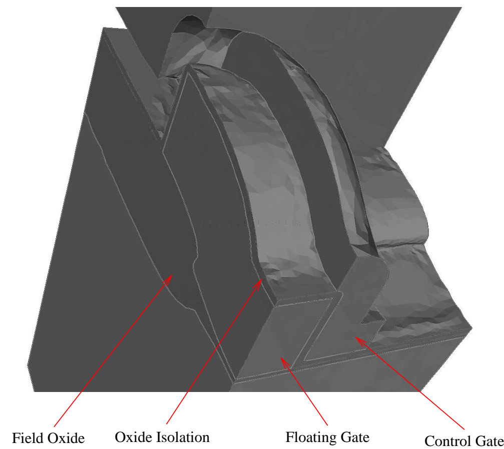

Figure 4: Caywood-EEPROM memory cell generated by three-dimensional process simulation

The process simulation flow is continued by the deposition of a poly-silicon layer for the control gate. Therefore the isotropic deposition model is again applied with a lower cellular resolution since the layer thickness is relatively large. Then the formation of the control gate is carried out by applying the empirical etching model in combination with the aerial image based mask modification.

Finally the structure is completed by depositing a thick layer of silicon dioxide. The simulation of this last process step is carried out by the empirical planarization model of TOPO3D which simply puts a planar layer on top. As well

as the empirical etching model the planarization model is very efficient concerning computational effort and is sufficient to obtain an appropriate result.

4 Results

Figure 4 shows the final device structure generated by the process simulation. Due to symmetry just one quarter of the memory cell is analyzed. This structure is used to extract the coupling capacitance between the gates, which is one of the most important factors for EEPROM-Cell programming. The capacitance extraction is performed with the finite element based SAP package [7], which is capable of acquiring all partial capacitances between conductors (semiconductors), namely the gates and the silicon bulk. On the basis of these data the coupling ratio can consequentially be derived by

$$K = C_{CG-FG}/(C_{FG-Si} + C_{CG-Si} + C_{CG-FG}). \tag{1}$$

For the memory cell shown in Figure 4 the extracted capacitances are

C_{CG-FG}	Control G. ↔ Floating G.	$2.38\cdot10^{-15}$F
C_{FG-Si}	Floating G. ↔ Bulk	$5.69\cdot10^{-16}$F
C_{CG-Si}	Control G. ↔ Bulk	$3.37\cdot10^{-16}$F

which results in a coupling ratio of $K = 72.4\%$.

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References

[1] J. M. Caywood, C. J. Huang, and Y. J. Chang, IEEE Trans.Electron Devices **49**, pp. 802–807 (2002).

[2] A. Hössinger, T. Binder, W. Pyka, and S. Selberherr, in *Proc. Intl. Conf. on Simulation of Semiconductor Processes and Devices* (2001), pp. 424–427.

[3] DIOS-ISE, *ISE TCAD Release 9.0*, ISE Integrated System Engineering AG, Zürich, Switzerland, 2003.

[4] W. Pyka, R. Martins, and S. Selberherr, in *Proc. Intl. Conf. on Simulation of Semiconductor Processes and Devices*, (1998), pp. 16–19.

[5] A. Hössinger, J. Cervenka, and S. Selberherr, in *Proc. Intl. Conf. on Simulation of Semiconductor Processes and Devices* (2003), pp. 259–262.

[6] H. Kirchauer and S. Selberherr, in *Optical Microlithography XI*, edited by L. V. der Hove (SPIE, 1998), pp. 764–776.

[7] R. Sabelka and S. Selberherr, in *Proc. Intl. Interconnect Technology Conference* (1998), pp. 250–252.