Simulation of the failure mechanism of power DMOS transistors under avalanche stress

A. Icaza Deckelmann*, G. Wachutka*, J. Krumrey**, F. Hirler**

*Institute for Physics of Elecrotechnology, Munich University of Technology,
Arccisstr. 21, D-80290 Munich, Germany
icaza@tep.ei.tum.de, wachutka@tep.ei.tum.de

**Infineon Technologies AG,
Balanstr. 73 D-81541 Munich, Germany
joachim.krumrey@infineon.com, franz.hirler@infineon.com

Abstract

The failure mechanism caused by avalanche stress in power devices consisting of large DMOS cell arrays is investigated using electrothermal device simulation. To this end, we use the approximation of an infinitely large array, but allow for thermal interaction among the cells. The numerical analysis demonstrate the occurrence of unstable states, where a single hot spot and a current filament evolve in one particular 'weak' cell, thus confirming earlier work. We also demonstrate that the maximum temperature rise in the first cell exhibiting filamentary current flow can easily exceed the destructive level. Subsequent current and temperature redistributions observed in simulation thus turn out to be of no practical relevance.

1 Introduction

In previous work, the mechanism underlying the failure of power DMOS transistors under avalanche operating conditions has already been addressed [1]. The devices under consideration, which consist of a large array of DMOS cells in parallel with common terminals, were approximated by an equivalent circuit, consisting of identical cells electrically connected in parallel, but without thermal interaction (fig. 1). Using this approximation and by focusing on one single cell contained in the array, it was possible to employ electrothermal device simulation to analyze the failure mechanism of the cell array induced by an applied current step. With this model, we obtained good agreement with measured data up to high current densities.

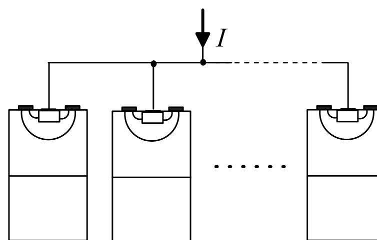

Figure 1: Multiple DMOS cells connected in parallel.

The simulations revealed that, initially, the device current is periodically distributed in the array, but concentrates on a single cell after a critical level of the maximum temperature inside the cell, T_{max}, has been exceeded. As a consequence, current filamentation

and relocation of the hot spot were observed in this particular cell, leading to unstable behavior of the cell array and to eventual device failure. In this work, we performed simulations of a small cell array, with thermal interaction between neighboring cells properly included, and demonstrate, for the first time, that indeed negligible thermal cross-talk occurs among the cells until a critical temperature is attained, and that after that the total current of the array rapidly concentrates onto a single cell. In particular, the time and the temperature level at which this redistribution of the current density sets on agrees well with the values predicted by a single-cell simulation. Thus, the model assumed so far has been corroborated, leading us to the conclusion that results from single-cell simulations can be transferred consistently to cell arrays.

2 Simulation Model

The real industrial device consists of a large array of DMOS cells electrically connected in parallel, and integrated on a silicon chip. The border of the active chip area consists of cells of similar geometrical design, but working as diodes. They are also connected in parallel to the transistor array. The regular DMOS cells outnumber the border cells by a factor of about 1000; thus, for safe operation it is mandatory that the current is uniformly distributed over the whole active chip area.

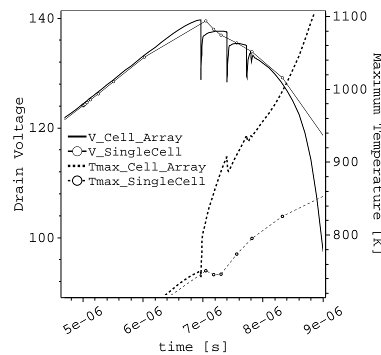

Figure 2: Voltage and temperature transients for single-cell and multiple-cell simulation of an applied current step.

For a realistic electrothermal device model, the proper choice of the thermal boundary conditions is of decisive importance for correct modeling. The thermal contact as encountered on the bottom side of the real devices bottom side as well as the high thermal resistance associated with the top side can be accurately implemented in our simulation model.

However, the boundary conditions for heat transport along the lateral borders of the chip and, hence, their effect on the temperature distribution cannot be included in the simulation model at acceptable computational expense, since this would require to perform an electrothermal simulation for 10^5 cells. But solving the heat transport equation with the approximation of a volume heat source [2] indicates that the temperature will be almost homogeneous over the active chip area, except for small stripes of width W along the borders, where $W \simeq L_{th} = \sqrt{D_{th} \cdot t}$; L_{th} = thermal diffusion length, D_{th} = thermal diffusivity, t = time elapsed. For the time range to be investigated, W amounts to a small portion of the lateral extension of the chip. Therefore we may approximate the interior of the DMOS array by a block consisting of a small number of cells, which do not exchange heat with the rest of the array. Consequently, we may assume reflecting boundary conditions along the borders. The cells contained in the simulation block, on the other hand, are allowed to interact electrically and thermally. It shall be noted that traveling-filament solutions cannot be found with this approach.

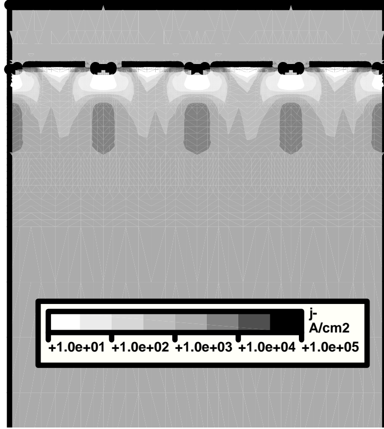

Figure 3: Electron current density in the simulated cell array before critical temperature is reached ($t = 6, 9\mu s$).

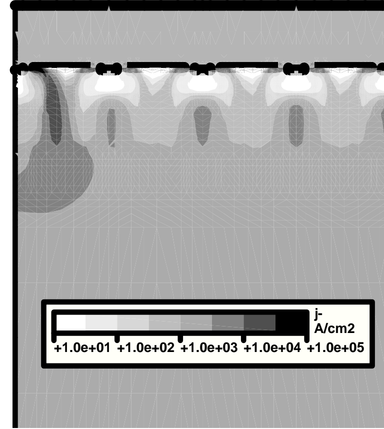

Figure 4: Electron current density in the simulated cell array after critical temperature is reached ($t = 7, 1\mu s$).

3 Results

Fig. 2 displays the transients of the applied voltage and of the maximum temperature in the device as response to an applied current step. The simulations were performed for a single cell and for an array of 4 cells, corresponding to the description given in section 1, keeping the current per cell constant. A peculiar kink in $V(t)$ is observed in the single cell simulation, while for the same elapsed time t the voltage sustained by the 4-cell array drops rapidly. At this point in time, $T_{max}(t)$ reaches a critical level and displays an inflection. This is associated with a relocation of the hot spot in the interior of the the single cell [1]. In the 4-cell block, however, a fast increase of T_{max} becomes apparent. Subsequently, in the cell array, oscillations in $V(t)$ and $T(t)$ appear; however, the temperature is already high enough to produce damage to the metal layers on top of the device. Thus it can be concluded that these oscillations will not be observed in reality, when a large number of cells interact. Although, in the present simulation, the cells are allowed to interact electrically and thermally, the results are essentially the same as those obtained without thermal interaction [1]. This confirms the validity of the simulation setup with isolated cells as a tool to investigate DMOS device failure under avalanche stress conditions.
Fig. 3 shows the electron current distribution in the simulated 4-cell array at $t = 6, 9\mu s$, shortly before the dramatic temperature rise takes place. A periodic current distribution is observed within the array. After the steepening of $T_{max}(t)$ in fig. 2, a current filament has developed in one cell (fig. 4). The temperature distribution evolves in analogous manner: while originally of spatially periodic nature (fig. 5), it later reveals the existence of a single hot spot, at the same location as that of the current filament, as can be seen by comparison of figures 4 and 6, which correspond to the same elapsed time.
The results obtained from the single-cell simulation have been validated with reference to measurements on real devices, yielding a good agreement [1] (figure 7).

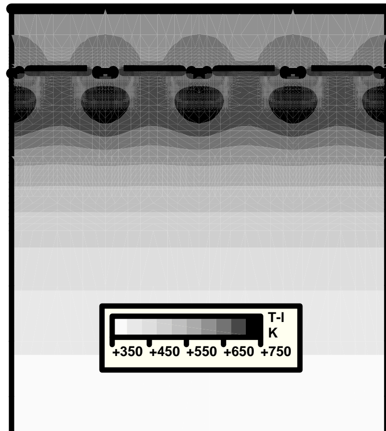

Figure 5: Temperature distribution in the simulated cell array before critical temperature is reached $(t = 6,9\mu s)$.

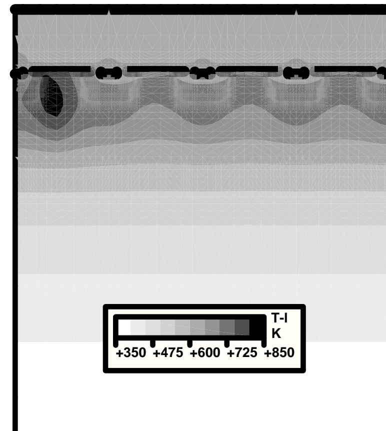

Figure 6: Temperature distribution in the simulated cell array after critical temperature is reached ($t = 7,1\mu s$).

4 Conclusions

An appropriate model for the electrothermal simulation of devices consisting of DMOS cell arrays under avalanche stress conditions has been presented. It takes into account proper boundary conditions for heat transport, assuming a quasi homogeneous temperature distribution over a large portion of the active device area, based on the characteristic thermal length. The thermal interaction of the simulated cells had no significant effect, thus justifying the assumption of isolated cells in parallel, and even of single cells to predict the operating limits of the devices. This is also corroborated by measured data. Current crowding and filamentation has been confirmed as basic failure mechanism, which was already ascertained in previous work [1].

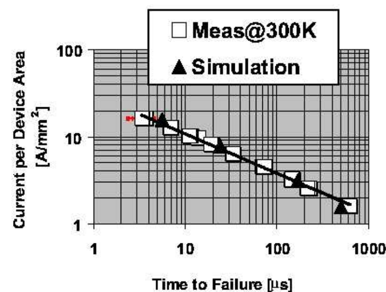

Figure 7: Comparison of measurement and simulation: applied current j_f vs. time-to-failure t_f.

References

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[2] N. Rinaldi, “Thermal analysis of solid-state devices and circuits: an analytical approach”, Solid State Electronics 44 (2000), pp. 1789-1798, Elsevier Science Ltd.