Optimal Contact Placement in Partially Depleted SOI with Application to Raised Source-Drain Structures

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Abstract

We have studied the impact on drive current of bringing the S/D contacts closer to the gate edge. We found that there is an optimal location for contact placement beyond which Idsat decreases. The decrease in Idsat is due to two phenomena: i) current crowding and ii) increase in contact resistance. We show that raised S/D structure will be able to circumvent these problems and allow for further improvement in drive current.

1 Introduction

Careful optimizations of all technology parameters have allowed conventional CMOS scaling to still achieve increasing performance. In this work, we focus on finding the optimal placement for source and drain contacts that maximizes drive current. In particular, we explore the impact on device performance of bringing such contacts closer to the gate edge. We show that there is indeed an optimal location and we explain the reasons for it.

2 Simulation Structures and Assumptions

Fig. 1 shows a cross section of the partially depleted SOI structure that we have considered in our study. Its dimensions and performance meet the ITRS roadmap predictions at the 90nm technology node. The specific topography and doping distribution are obtained from process simulations using the Synopsys simulation tool set [1] with parameters tuned to provide agreement to measured extension and deep S/D sheet resistances. The device characteristics at different contact locations are obtained from corresponding device simulations calibrated to baseline experimental data. Simulations were performed using two different contact models: 1) *lumped* and 2) *doping-dependent* distributed contact model. In the lumped one, the contact-to-silicon interface resistance is modeled by using a constant resistance in series with the contact, whereas the doping dependent distributed model uses a group of distributed resistances, which depend on the local doping concentration. [2].

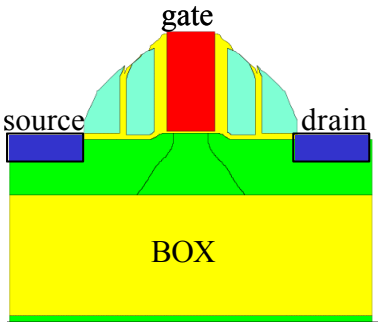

Fig. 1: Cross section of the Partially Depleted SOI simulation structure.

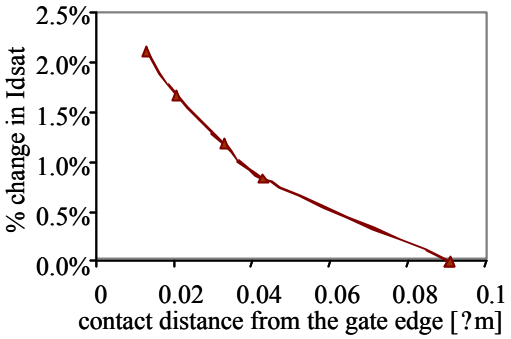

Fig. 2: Percentage change in Idsat as a function of contact location for box shaped contact using lumped model.

3 Results and Discussions

The core of our analysis centers on tracking changes in drive current as we increase the proximity of the S/D contacts to the gate edge. In all simulations we have kept device leakage, Vt, overlap capacitance, and other device characteristics constant, so that changes in drive current are fully representative of the drive capability of the devices. Initially we used simplistic ohmic box-shaped contacts, 300 Angstroms deep, to mimic the silicided region (Fig. 2) [3]. Since these results are based on the lumped contact model, the increase in Idsat is solely due to the reduction in S/D spreading resistance. Idsat monotonically increases with decreasing distance between the gate edge and the contacts. However, when using the doping-dependent model, as in Fig. 3, the scenario changes considerably. Here we compare the same box-shaped contacts to more realistic rounded-edge contacts. The trends clearly show that there is an optimal location, which maximizes drive current. It also shows that the decrease in Idsat past the optimal point is more significant for the box-shaped contact than for the rounded-edge one. To explain the reasons behind it, we looked at the current flow lines in light of the contact resistance as a function of doping. We see (Fig. 4) that as the doping concentration drops below 1e20 cm^{-3}, the contact resistance increases dramatically. Therefore, as we move the contact closer to the gate edge, as from Fig. 5a to Fig. 5b, the current starts to crowd around the bottom edge of the contact to avoid the highly resistive contact interface, and is thus forced through the lower-doped part of the doping profile. This behavior is even more prominent for the boxed-shaped contact (Fig. 6a and 6b). The exact balance of these two competing effects, the gain from the reduction in spreading resistance and the loss due to current crowding, determines for each given technology the exact optimal contact location.

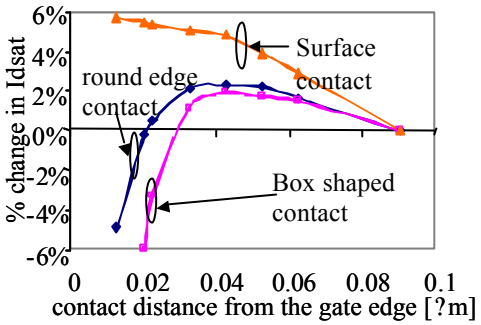

Fig. 3: Percentage change in Idsat as a function of contact location using doping dependent model.

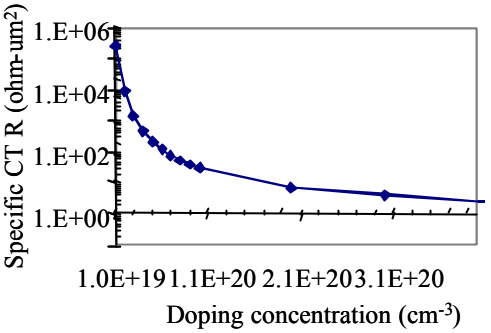

Fig. 4: Specific contact resistance (ohm-mm^2) as a function of doping concentration.

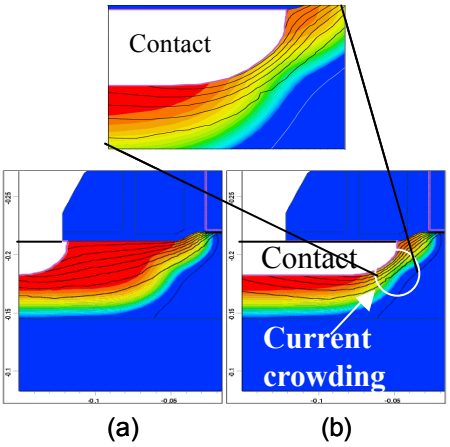

Fig. 5: Current flow lines and doping profile for rounded-edge contact.

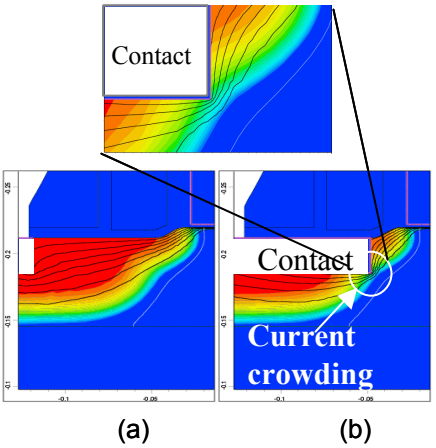

Fig. 6: Current flow lines and doping profile for box-shaped contact.

To minimize the current crowding and thus further improve device performance, contacts would need to be shallow enough not to land on a low doping concentration region. In other words, they would need to be like our surface contacts in Fig. 7a and 7b. Unfortunately, silicon consumption during the silicidation process is inevitable. One way to circumvent the problem would be the usage of raised source and drain regions [4]. Fig. 8a and 8b show the current flow lines for 300A thick raised S/D regions, and indeed the

flow lines are similar to our previous surface contact case with the current crowding being absent. As a result the device drive current keeps on increasing as the contact is moved closer to the gate edge (Fig. 9).

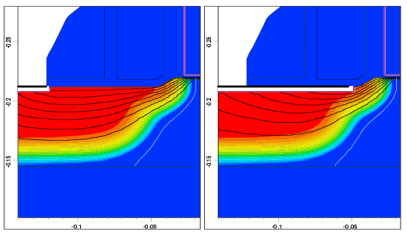

Fig. 7: Current flow lines and doping profile for surface contact.

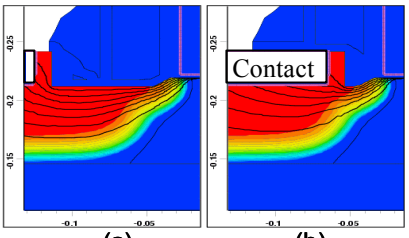

Fig. 8: Current flow lines and doping profile for raised S/D with box-shaped contact.

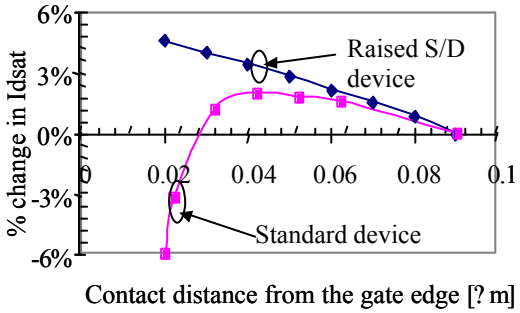

Fig. 9: Comparison of percentage change in Idsat as a function of contact location obtained using doping dependent box shaped contact model for raised S/D and Standard device.

4 Conclusions

We explored the impact on drive current when the S/D contacts are brought closer to the gate edge. We found that there is an optimal location for contact placement. Based on our analysis we predict that raised S/D with optimized contact placement will provide drive current improvement.

5 References

[1] Taurus-Tsuprem4 and Taurus-Medici, version 2003.12, Synopsys.
[2] K. Varahramyan et al., SSE, Vol. 39, No. 11, pp. 1601-1607 (1996).
[3] L. Su et al., ED letters, Vol. 15, No. 9, pp. 363-365 (1994).
[4] W. Jeamsaksiri et al., ED transactions, Vol. 50, No. 3, pp. 610-617 (2003).