Optimization of Recessed and Elevated Silicide Source/Drain Contact Structure Using Physical Compact Resistance Modeling and Simulation in Ultra-Thin Body SOI MOSFETs

Seong-Dong Kim*, Jeffrey B. Johnson*, Jun Yuan**, and Jason C.S. Woo**

*IBM Systems & Technology Group, Essex Junction, VT 05452, USA
sdkim@us.ibm.com, jbj@us.ibm.com

**Electrical Eng. Dept., University of California, Los Angeles, CA 90024, USA
jun_yuan@icsl.ucla.edu, woo@ee.ucla.edu

Abstract

Optimization of source/drain (S/D) extrinsic resistance of ultra-thin body (UTB) silicon-on-insulator (SOI) MOSFETs with recessed and/or elevated silicide contact structure is investigated through new simplified physical compact modeling and 2-dimensional simulation calibrated with 90-nm SOI technology. It is found that the optimum silicide contact can be located below SOI layer surface in elevated contact structure if effective contact length is highly scaled. The closed-form analytical expressions provide a simple guideline for silicide contact design with respect to SOI thickness and contact length in self-aligned silicide technology.

1 Introduction

Ultra-thin body SOI MOSFETs are of great interest for low power and high speed applications because of their excellent short channel behavior even with an undoped channel. However, the sophisticated S/D self-aligned silicide contact technologies such as elevated (or raised) S/D or fan-out S/D structures are highly desirable due to high extrinsic parasitic resistance. It is generally thought that as the silicide consumption of silicon increases, the contact series resistance is susceptible to increase due to the decrease in active dopant concentration at the silicide/Si interface or increase in sheet resistance underneath silicide ($R_{sh,co}$) [1]. Besides, the resistance associated with the current injected from the sidewall edge of recessed silicide contact has been excluded in resistance estimation because of its small contribution [2]. However, in highly scaled nanoscale CMOS devices, this additional parallel resistance component of sidewall contact may become comparable to the resistance of diffusion layer under planar silicide contact as the effective contact length, L_{con} (which is defined as a length from sidewall spacer edge to the contact plug edge) is scaled to less than ~150 nm, leading to different series resistance behavior with respect to silicide thickness or contact location. In this paper, we examine the optimization of the S/D extrinsic resistance for the recessed and elevated S/D silicide contact structure through physical compact modeling and 2-dimensional TCAD simulation. A new simplified physical compact modeling is developed and applied to 90-nm SOI CMOS technology to investigate the sub-resistance component contribution and parameter sensitivity. The model-based guideline for the optimum location of silicide/Si interface in elevated S/D structure is proposed with respect to the device parameters including contact size and SOI thickness.

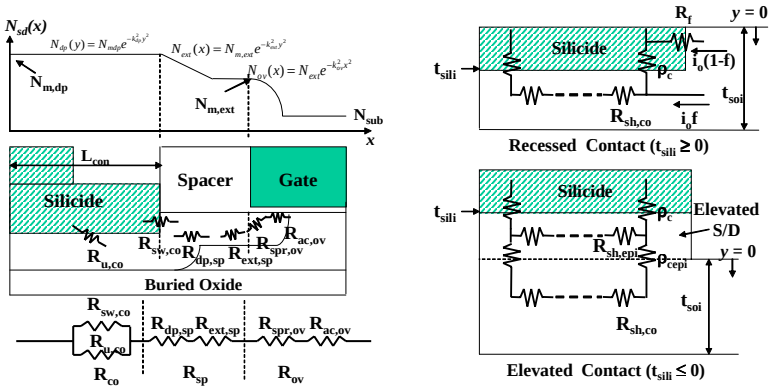


Figure 1: (a) Schematic representation for physical compact modeling of S/D extrinsic resistance and (b) recessed and elevated silicide contact cross-section with modified tri-layer TLM network model.

2 Compact Extrinsic Resistance Modeling

The total extrinsic resistance can be divided into three sub-resistance components by regional group as illustrated in Fig 1(a): The resistance in S/D extension-to-gate overlap, R_{ov}; the resistance under sidewall spacer, R_{sp}; the resistance in silicide-diffusion contact region, R_{co}. The simple compact model for overlap resistance is analytically developed using 1-radian current spreading angle [3], current spreading point as a fitting parameter and surface potential expression with average Gaussian doping. The total current flow towards recessed silicide contact is modeled by two parallel current components ($t_{sili} \geq 0$); One is a current component at the edge of the silicide contact ($R_{sw,co}$) and the other is at silicon layer underneath silicide ($R_{u,co}$) as shown in Fig. 1(b). For the elevated contact structure ($t_{sili} \leq 0$), the modified 1-dimensional tri-layer transmission line model (1-D TLTLM) principle [4] is adopted by using effective resistive descriptions of horizontal and vertical current components. The contact resistances comprising the current flow effect in the sidewall contact of a recessed silicide, and also in the elevated S/D contact structure are expressed as

$$R_{co} = \left(R_{u,co}^{-1} + R_{sw,co}^{-1}\right)^{-1} \quad \text{for} \quad t_{sili} \geq 0 \tag{1}$$

$$R_{co} = \frac{R_{sh,co}}{\rho_{cepi}(G^2 - F^2)}\left(\frac{R_{sh,co} - \rho_{cepi}F^2}{G\tanh(GL_{con})} - \frac{R_{sh,co} - \rho_{cepi}G^2}{F\tanh(FL_{con})}\right) \quad \text{for} \quad t_{sili} \leq 0 \tag{2}$$

where ρ_{cepi} is effective coupling specific resistance of elevated S/D layer between silicide and SOI layer, and F and G are the functions of contact parameters [4].

3 Optimization of Silicide Contact Resistance

In order to investigate and predict resistance behavior with underlying physics as a function of various source/drain parameters, the model is calibrated with input parameters based on calibrated process simulation, device cross-section TEM and extracted resistance. Fig. 2 shows measured S/D extrinsic resistance data of 90-nm node SOI NMOSFET with recessed silicide contact for model and simulation calibration. The parameter sensitivity is analyzed by focusing on recessed silicide contact parameters such as effective contact length and silicide thickness due to the dominant R_{co} contribution (> ~50%) as shown in Fig. 3. The optimization through modeling and simulation is also applied to the elevated S/D contact structure and the

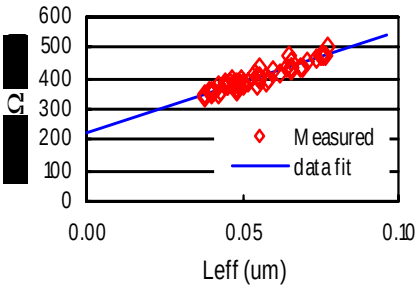


Figure 2: Measured S/D extrinsic resistance data of NMOSFET for model calibration and TCAD simulation.

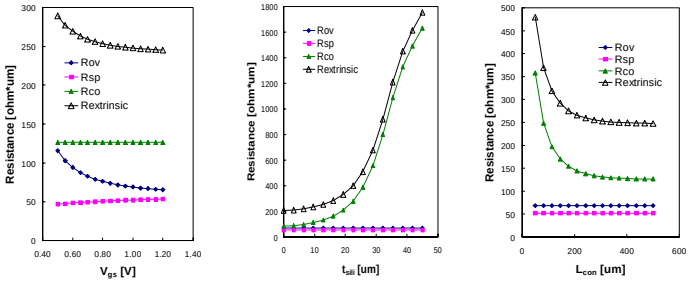
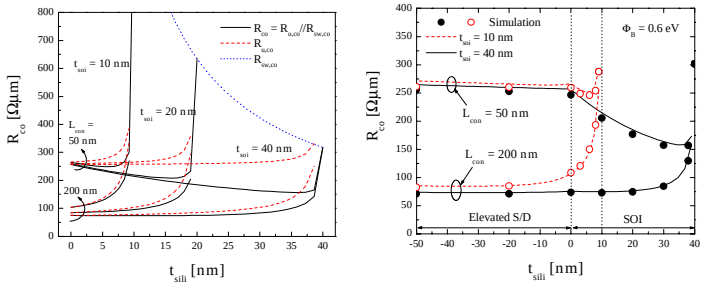


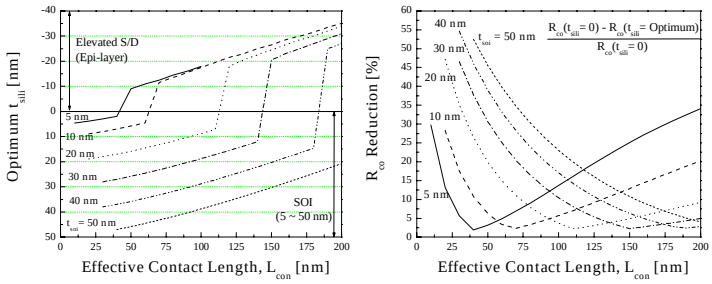
Figure 3: Modeling analysis of S/D extrinsic resistance and components calibrated with measured and simulation data. Significant R_{co} contribution (> 50%) is observed.

different resistance trends with respect to contact length range are observed as shown in Fig. 4(a), i.e., R_{co} increases as t_{sili} increases for long contact case (L_{con} = 200 nm) due to the dominant effect of current flow under the silicide contact [2]. However, in the case of relatively short contact (L_{con} = 50 nm), the contact resistance component ($R_{u,co}$) in Si-layer under silicide becomes larger compared with the resistances in the sidewall contact ($R_{sw,co}$), so that $R_{sw,co}$ gradually takes effect on the total contact resistance as recessed t_{sili} increases. It should be noted that there is an optimum silicide contact location in thin-film SOI layer for extremely scaled UTB SOI MOSFET with relatively short contact size. This phenomenon and the derived analytical expression are verified by 2-D device simulation in Fig. 4(b) and found to be in good agreement with various conditions by changing the doping, specific contact resistance, contact length, and SOI thickness. Fig. 5(a) and (b) show the modeling prediction of optimum silicide/Si interface location as a function of effective contact length in elevated S/D contact structure and the resistance improvement rate at optimum t_{sili} with respect to at t_{sili} = 0 nm, respectively. It is interesting to note that the optimum t_{sili} doesn't necessarily lie at the interface of elevated S/D epi-layer/SOI or above, but can be located in the SOI region underneath, in case that contact diffusion doping is uniform and L_{con} is relatively short. The percentage of the resistance reduction at optimum t_{sili} is in proportion to t_{soi}. It can be also observed that the transition point of effective contact length, where the optimum location of silicide/Si interface is changed from elevated S/D layer to SOI region, is dependent on the contact parameters that determine contact transfer length such as Schottky barrier height, doping concentration, doping profile shape, and SOI thickness. In 30 nm-thick SOI case, the optimum silicide/Si interface position is located below the center point of t_{soi}, when L_{con} is less than ~ 140 nm as shown in Fig. 5(a). This implies that the expensive and difficult elevated S/D process may not be needed if an advanced silicide process which enables aggressive scaling of silicide



(a) (b)

Figure 4: (a) Contact resistance behavior according to effective contact length and (b) its simulation verification for elevated contact with t_{soi} = 10 and 40 nm.



(a) (b)

Figure 5: (a) Guideline for optimum silicide contact location as a function of effective contact length in elevated S/D contact structure and (b) resistance improvement at optimum t_{sili} with respect to t_{sili} = 0 nm.

consumption of silicon is successfully developed. Furthermore, we can mitigate large parasitic gate-to-S/D capacitance drawback of elevated S/D structure by reduction of the elevated layer thickness through optimization. This transition point shifts to a lower value when the contact transfer length is decreased by lower specific contact resistance, non-uniform doping profile or lower SOI thickness.

4 Conclusion

A simple and efficient guideline for determining the optimum silicide thickness and contact parameters of UTB SOI CMOS with recessed or elevated contact structure is proposed. A significant contribution of contact resistance component is confirmed by the physical modeling and simulation analysis calibrated using experimental data of nanoscale SOI technology. The resistance behavior and optimum silicide contact location are found to depend on contact length and UTB SOI layer thickness.

References

[1] L.T. Su, M.J. Sherony, H. Hu, J.E. Chung, D.A. Antoniadis, "Optimization of series resistance in sub-0.2 μm SOI MOSFET's," *IEEE EDL*, vol. 15, pp. 363-365, Sept. 1994.

[2] B.-Y. Tsui, and M.-C. Chen, "Series resistance of self-aligned silicided source/drain structure," *IEEE Trans.Electron Devices*, vol. ED-40, pp. 197-206, Jan. 1993.

[3] K.K. Ng and W.T. Lynch, "Analysis of the gate-voltage-dependent series resistance of MOSFETs," *IEEE Trans. Electron Devices*, vol. ED-33, pp. 965-972, July 1986.

[4] G.K. Reeves and H. B. Harrison, "An analytical model for alloyed ohmic contacts using a trilayer transmission line model," *IEEE Trans. Electron Devices*, vol. ED-42, pp.1536-1547, Aug. 1995.