

# SPICE-Compatible Macro Model for Split-Gate Compact NVM Cell with Various Gap Sizes

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## Abstract

In this paper we present a SPICE-compatible macro model based on three MOS transistors to describe split-gate non-volatile memory (NVM) cell characteristics for various sizes of the gap between the gates. The model has initially been developed based on simulated dc-IV-characteristics of reference cells (floating gate connected to control gate) and was verified later with measurements on reference as well as real floating gate cells.

## 1 Introduction

The development of a SPICE-compatible macro model of the compact NVM cell [1] (see Fig.1), which is a split-gate cell type and a candidate for embedded flash memories in advanced CMOS technologies, is needed to allow memory designers to simulate and compare different memory circuits in an early phase and to optimize them e.g. for low power consumption. Sim et al. [2] presented a macro model to describe the characteristics of a split-gate cell based on a 2 MOS transistors model. Nevertheless, no attention has been paid to describe the influence of the gap, which is meant to isolate the floating gate from the access gate, on the memory characteristics. The effect of the gap size becomes more significant for next flash technologies due to gate length and supply voltage reduction and to the fact that the gap will not scale too much in order to avoid breakdown when a high control gate voltage is used, e.g. during erase operation. In this paper the influence of the isolation spacer on the dc-characteristics of the compact cell is presented and modeled using an extra transistor in the macro model for a more accurate description of the memory characteristics. This extra transistor mimics the non-gated channel region under the gap.

## 2 Effect of the Gap Size on Memory Performance

The gap width has a relevant impact on the memory performance e.g. read current, program/erase voltage, reliability etc. Calibrated TCAD simulations have been used to predict the impact of the gap size on the read current, see Fig. 2. The read current increases by a factor of 2.5 when the gap is reduced from 65 to 35 nm. However, simulations predict a saturation level of the read current when the gap becomes thinner than about 20 nm. Unfortunately, for thin isolation spacers, the parasitic coupling of the access gate (AG) reduces the essential capacitive coupling between CG and FG, and

hence, the program and erase gate voltage increases [3]. Moreover, the breakdown voltage of the gap between CG and AG decreases, and the reliability of the device could be affected. Accordingly, the isolation spacer in the compact cell should be thicker than 20 nm, and a macro model should be able to describe the effect of the spacer width on the characteristics of the compact cell.

### 3 Macro Model

In the development of a macro model for the compact cell, we focused our attention first on the dc-modeling, e.g. steady-state I-V characteristics including drain current during read and source side injection (SSI) write operations, of a reference cell in order not to obscure the dc-modeling by the capacitive coupling between FG and other terminals. Rather than developing a single new compact model, we made use of a compound model approach in order to describe the memory cell by a sub-circuit of existing compact models. We tried first to model the cell by using a two MOS transistors scheme (see Fig. 3) describing the AG and FG transistors. The MOS transistors are modeled by MOS model 11 (MM11) [4]. In this two transistors scheme it is assumed that the impact of the gap section can be neglected with respect to the series combination of the AG and FG. In order to obtain a first estimate for the MM11 parameters for both MOSFETs, stand-alone variants of the AG and FG have been simulated (using Medici) and the MM11 parameters have been extracted from the Medici simulated I-V characteristics. The results of the macro model with 2 transistors scheme agreed well with Medici simulations (given in table 1) for a 10 nm gap but significant deviation was observed for 20 nm gap (see Fig. 4A) and wider. This suggests that the gap section could not be neglected, and should be taken into account. By interpreting the gap section as a third MOS transistor “SG” (see Fig. 3), modeled by MM11, more accurate results are obtained (see Fig.4B). Most of the MM11 parameters of the spacer transistor have been taken as the average of the AG and FG value. The gate bias of SG was taken  $(V_{AG}+V_{FG})/2$ .

### 4 Model Verification and Conclusion

Measurements (given in table1) have been performed on reference cells as well as real floating gate cells. The FG/CG and AG lengths are 165 and 175 nm respectively (from SEM and electrical measurements). The gap size is 35 nm. The coupling coefficients of the CG ( $\alpha_{CG}$ ), AG ( $\alpha_{AG}$ ), and the FG voltage due to initial charges ( $Q_f/C_t$ ), where  $C_t$  is the total capacitance of the FG, have been extracted by comparing the dc-characteristics of FG and reference (contacted FG) compact cells and found to be  $\alpha_{CG}=0.52$ ,  $\alpha_{AG}=0.15$ , and  $Q_f/C_t=-0.17V$ . MM11 parameters of the representative 3 MOS transistors of the reference cell have been extracted as discussed in section 3, and electrical results of the macro model are compared to measurements as shown in Fig. 5. A very satisfactory fit is obtained. In Fig. 5, we focused on the sub-threshold characteristics of the AG transistor rather than on those of the FG transistor since, in a common ground NOR-type array configuration, the AG is used as a switch to select a specific cell during read and program. Any sub-threshold current leakage of the AG will therefore affect unselected cells, resulting in read and write disturbs.

Subsequently, the model was extended to fit the characteristics of real FG cells by making use of the extracted coupling coefficients. Results are shown in Fig. 6. Again, a good fit is obtained indicating high accuracy in the coupling coefficients extraction method. In summary, a SPICE-compatible macro model based on three MOS transistors has been developed and verified to model the drain current in read and SSI write operations of a split-gate cell with various gap sizes. The model can serve as a basis for accurate memory circuit simulations.

## References

- [1] M. van Duuren et al., "Compact poly-CMP embedded flash memory cells for one or two bit storage," in *Proc. NVSMW*, pp. 73-74, 2003.
- [2] S-P. Sim et al., "Parameter and coupling ratio extraction for SPICE-compatible macro modeling of source side injection flash cell", *Proc. SISPAD*, pp.356-359, 2001.
- [3] M. Slotboom et al., "Gate isolation technology for compact poly-CMP embedded flash memories", in *Proc. ESSDERC*, pp.159-163, 2003.
- [4] [www.semiconductors.Philips.com/Philips\\_Models](http://www.semiconductors.Philips.com/Philips_Models)

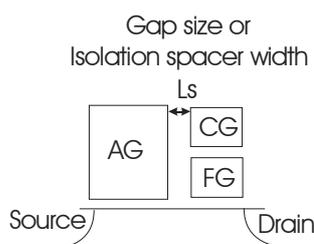


Figure 1: Compact NVM cell. The reference cell has the floating gate (FG) electrically connected to the control gate (CG). AG is the access gate transistor.

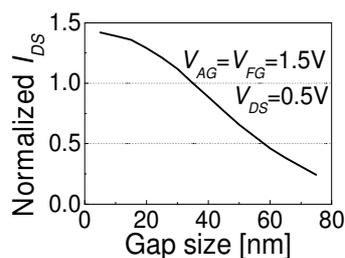


Figure 2: Simulation of the effect of the isolation spacer width on the read current of the compact cell. The AG and FG length are  $L_{AG}=0.2\mu\text{m}$ ,  $L_{FG}=0.12\mu\text{m}$ .

	Device Simulation Conditions
a	$I_D-V_{AG}$ at $V_B=0, -1$ and $-2V$ , $V_{FG}=2V$ , $V_{DS}=50\text{mV}$
b	$I_D-V_{AG}$ at $V_B=0, -1$ and $-2V$ , $V_{FG}=2V$ , $V_{DS}=2V$
c	$I_D-V_D$ at $V_{AG}=V_{FG}=1, 1.5$ and $2V$ , $V_B=V_S=0V$
d	$I_D-V_D$ at $V_{AG}=1, 2V$ , $V_{FG}=4, 6V$ , and $V_B=V_S=0V$

Table 1: Medici device simulations performed on a reference compact cell. The electrical behavior of AG is described by a & b in linear and saturation region. c and d describe the drain current under read and SSI write operations.

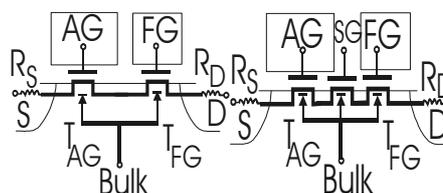


Figure 3: left) 2 MOS transistors scheme right) 3 MOS transistors scheme.

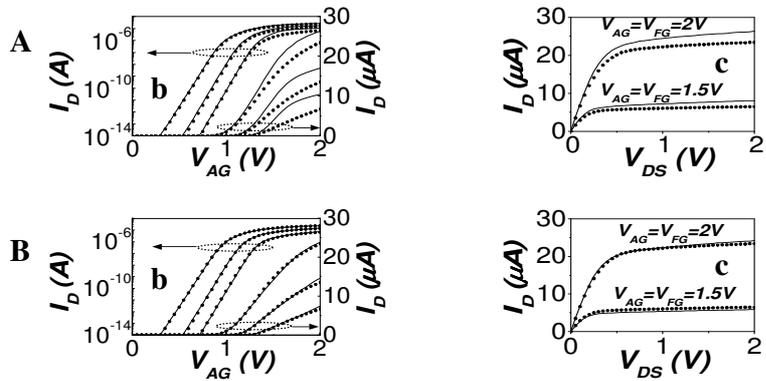


Figure 4: Medici device simulations (*symbols*) and compact model results (*lines*) for A) two-transistor B) three-transistor scheme as given in b and c in table1 for a compact reference cell with isolation spacer width  $L_S=20\text{nm}$ .

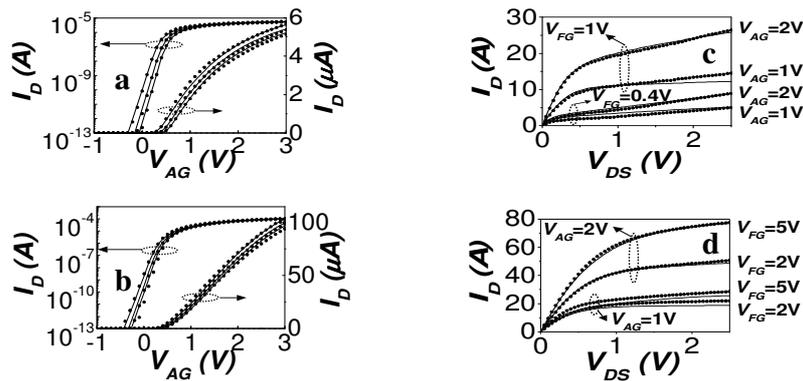


Figure 5: Measurements (*symbols*) and corresponding three-transistor compact model results (*lines*) as given in table1 (but with  $V_{FG}=V_{AG}=4V$  instead of 2V in a, b) for a compact reference cell (contacted FG) with spacer width  $L_S=35\text{nm}$ .

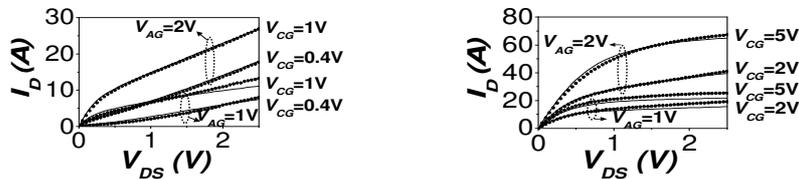


Figure 6: Measurements (*symbols*) and corresponding 3 transistors compact model results (*lines*) for a real FG compact cell.