Simulation Study of Simple CMOS-Compatible Thin-SOI Vertical Bipolar Transistors on Thin BOX with an Inversion Collector

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Abstract

A simulation study has been performed on CMOS-compatible, thin-SOI, silicon-base, vertical bipolar transistors as a potential solution for cost-effective SOI BiCMOS. These transistors have a virtual collector, which is an inversion layer created by the substrate bias. Device performance is suitable for mixed-signal applications, and scales well with design rules and SOI thickness.

1. Introduction

SOI BiCMOS is recognized as a preferred technology for mixed-signal design. Among the various types of bipolar transistors, a vertical bipolar affords higher performance than a lateral device, but its integration with thin-SOI CMOS is more complex and costly due to the thick sub-collector. Recently, a CMOS-compatible, thin-SOI, SiGe-base, vertical bipolar transistor with high performance has been demonstrated at the cost of SiGe epitaxy and several additional masks [1-3]. In this paper, we propose a very simple silicon-base vertical bipolar transistor on thin SOI that uses the SOI silicon layer as the base and an inversion layer as the collector. Conceptually, the device looks like a double-gated diode with a polysilicon emitter replacing the top gate and oxide, self-aligned to the extrinsic collector and extrinsic base using spacers. Potentially, its CMOS-like process facilitates a straightforward integration with high-performance thin-SOI CMOS. Device physics, device design and scaling are studied through simulation.

2. Device Concept

A cross-sectional schematic is shown in Fig.1. Two-dimensional device simulations are conducted in MEDICI [4]. The simulated device has an emitter stripe width (W_E) of 100 nm, a box-like base doping profile (N_B) of 2e18 cm^{-3} and a SOI thickness (T_{SOI}) of 50 nm. The emitter is n^{++} polysilicon. The spacing between the emitter and the n^{++} extrinsic collector (L_{sp1}) is 100 nm, while the spacing between the emitter and the p^{++} extrinsic base (L_{sp2}) is 50 nm. The buried oxide thickness is 10 nm. Preliminary experimental results suggest that the critical dimensions used in the simulations can be achieved. Fig. 2 and 3 show the Gummel plot and the output characteristics respectively, at V_{SE} = 3 V, which is a representative gate bias for a CMOS technology with T_{ox} = 10 nm [5]. The current gain (β) is above 230 over a wide range of the collector current. The Early voltage (V_A) is 102 V. At high V_{BE}, base widening occurs and a buildup of excess holes and electrons is observed throughout the SOI layer. The RF performance is extracted from small signal analyses, and is plotted at V_{SE} = 3 V in Fig. 4. f_T and f_{max} reach their peak values of 35 GHz and 118 GHz at I_C = 132 mA/mm, respectively.

The impact of the substrate bias on the RF performance is shown in Fig. 5, where the peak f_T and f_{max} are plotted vs. V_{SE}. Fig. 6 shows a vertical cut of the carrier concentration through the center of the emitter at the biases of V_{CE} = 3 V, V_{BE} = 0.86 V and V_{SE} = 0, 1 and 3 V. At V_{SE} < 1 V, the inversion layer is not formed at the back interface, and the device is a quasi-lateral BJT with the n^{++} region as the collector. At V_{SE} > 1 V, the inversion layer forms, and the device becomes a vertical BJT with the inversion layer as the collector, as seen in Fig.

7, where a 2D contour of the net carrier concentration at V_{SE} = 3 V is illustrated. The substrate bias creates both the inversion layer and a depletion layer above it, and it also acts like the bias on the virtual collector. As V_{SE} increases, the depletion layer gets wider and the inversion gets stronger, hence W_B reduces and r_b increases while r_c and C_{dBC} decrease. The net result is that f_T and f_{max} increase with increasing V_{SE}, as shown in Fig. 5. However, the increasing r_b slows down the enhancement in f_{max}, particularly at large V_{SE} values. Very high V_{SE} should be avoided in practice in order to prevent oxide breakdown and base-collector punchthrough. Furthermore, it is noted that V_{BE} also affects the depletion width and induced electron concentration. This is analogous to the body effect in a MOSFET, only that the body in our case is biased via a forward-biased p/n junction (E-B).

3. Device Design and Scaling

Since the intrinsic collector depends on the base doping concentration, the device design is mostly the base design. Fig. 8 shows the peak f_T and f_{max} vs. T_{SOI} for a fixed N_B of 3e18 cm^{-3}. f_T increases by 68% as T_{SOI} is reduced by half due to reduced W_B, hence reduced τ_B. However, f_{max} only increases by 38% because of r_b constraints. A similar trend has been observed in the peak f_T and f_{max} vs. N_B for a fixed T_{SOI} of 50 nm, as shown in Fig. 9. f_T increases significantly with decreasing N_B due to a widened depletion region, hence reduced C_{dBC} and W_B, while the enhancement in f_{max} is limited by r_b increase. Another device parameter is the length of the collector reach-through region, L_{sp1}. Reducing L_{sp1} can improve f_T by reducing r_c and lateral transit time. In order to prevent C-E punchthrough for small L_{sp1}, the base doping concentration near the extrinsic collector can be increased, e.g., by a one-sided halo implant. Such a design may enhance f_T but degrade f_{max}, as shown in Fig. 10. Therefore, various tradeoffs have to be made in the device design for different circuit applications.

As the device scales, conventional bipolar scaling rules can be used [6]. While the litho dimension is scaled by a factor of κ, W_B (not T_{SOI}) and N_B are scaled by a factor of $\kappa^{0.8}$ and $\kappa^{1.6}$, respectively. Meanwhile, the supply voltage is kept constant. f_T and f_{max} vs. I_C for devices with W_E = 200, 100 and 50 nm at V_{SE} = 3 V and V_{CE} = 3 V are shown in Fig. 11 and 12, respectively. All the other lateral dimensions are also scaled by κ = 2. It is noted that the peak f_T scales with $\kappa^{0.5}$ and the peak f_{max} scales with $\kappa^{0.8}$.

4. Conclusions

A simulation study has been performed on simple thin-SOI, silicon-base vertical bipolar transistors with a virtual collector. It outperforms lateral BJTs, while retaining the simplicity of fabrication. The performance scales well with the litho dimension using the conventional bipolar scaling rules. The CMOS-like process allows the direct integration of such devices with the current SOI CMOS technology, and therefore provides new opportunities for mixed-signal applications and circuit innovations.

References

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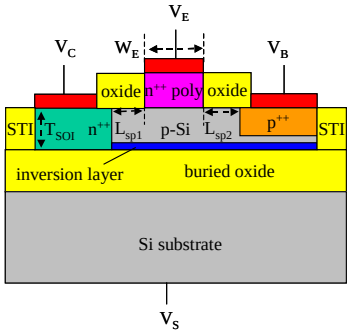

Fig. 1. Cross-sectional schematic of a vertical silicon–base npn BJT having an inversion layer as the collector on thin SOI substrate.

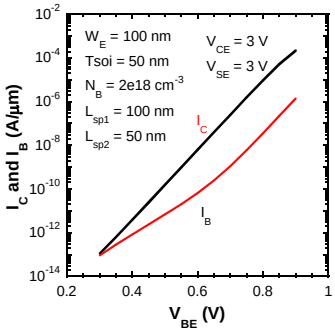

Fig. 2. Simulated Gummel plot for a device with W_E = 100 nm, T_{SOI} = 50 nm, N_B = 2e18 cm^{-3}, L_{sp1}= 100 nm, L_{sp2}= 50 nm and T_{ox} = 10 nm at V_{SE} = 3 V and V_{CE} = 3 V.

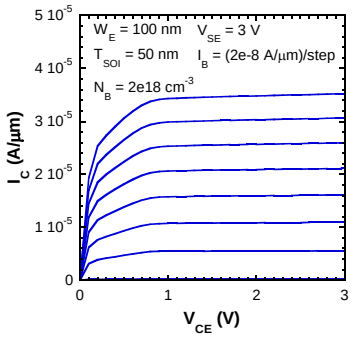

Fig. 3. Simulated output characteristics for the device in Fig. 2 at V_{SE} = 3 V.

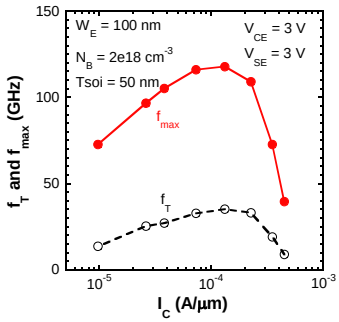

Fig. 4. Simulated f_T and f_{max} vs. I_C for the device in Fig. 2 at V_{SE} = 3 V.

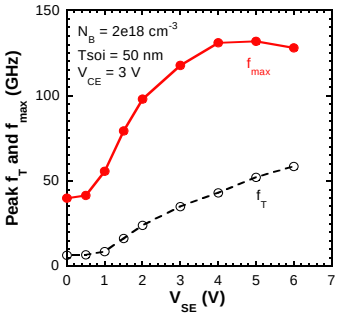

Fig. 5. Simulated peak f_T and f_{max} vs. V_{SE} for the device in Fig. 2 at V_{CE} = 3 V.

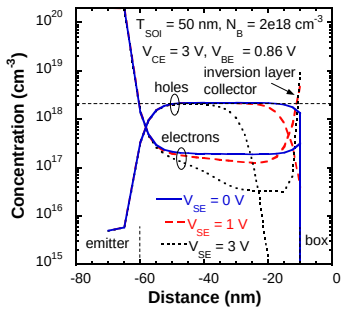

Fig. 6. 1D cut of carrier concentration through the center of the emitter for the device in Fig. 2 at V_{CE} = 3 V, V_{BE} = 0.86 V, and V_{SE} = 0, 1 and 3 V.

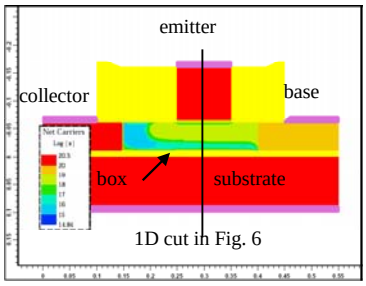

Fig. 7. Two-dimensional contour of the net carrier concentration for the device in Fig. 2 at V_{SE} = 3 V, V_{CE} = 3 V and V_{BE} = 0.86 V.

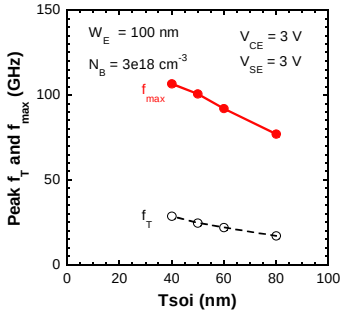

Fig. 8. Simulated peak f_T and f_{max} vs. T_{SOI} for devices with W_E = 100 nm and N_B = 3e18 cm^{-3} at V_{SE} = 3 V and V_{CE} = 3 V.

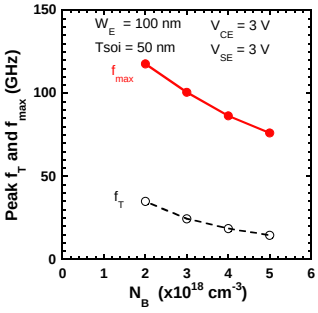

Fig. 9. Simulated peak f_T, f_{max} and V_A vs. N_B for devices with W_E = 100 nm and T_{SOI} = 50 nm at V_{SE} = 3 V and V_{CE} = 3 V.

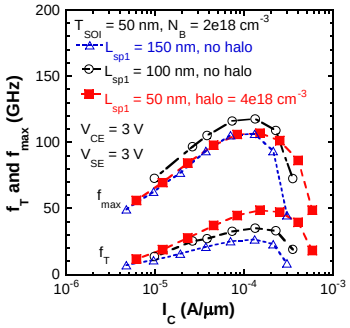

Fig. 10. Simulated f_T and f_{max} vs. I_C as a function of L_{sp1}. A halo with a box-like doping of 4e18 cm^{-3} and 25 nm in width is used for L_{sp1} = 50 nm to prevent punchthrough.

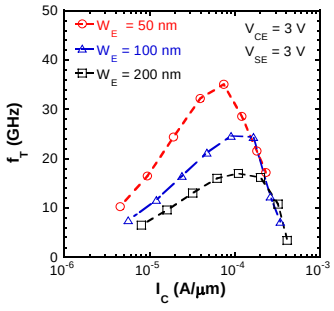

Fig. 11. Simulated f_T vs. I_C for scaled devices with W_E = 200, 100 and 50 nm, N_B = 1e18, 3e18 and 9e18 cm^{-3} and T_{SOI} = 90, 50 and 20 nm (W_B = 52, 30, 17 nm). All other lateral dimensions are scaled by 2x as well.

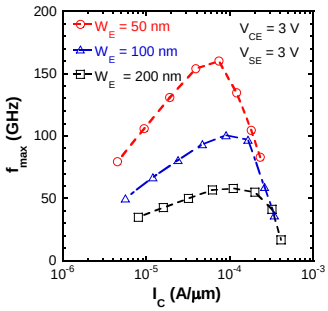

Fig. 12. Simulated f_{max} vs. I_C for scaled devices in Fig. 11.