

Investigation of a novel tunneling transistor by MEDICI simulation

P.-F. Wang, Th. Nirschl, D. Schmitt-Landsiedel, and W. Hansch

Institute for Technical Electronics, Technical University Munich
80333 Munich, Germany

pengfei.wang@tum.de, thomas.nirschl@tum.de, dsl@tum.de, hansch@tum.de

Abstract

For low power application, a semiconductor device with a low subthreshold leakage current is preferred. In this work a tunneling FET (TFET) with a reduced subthreshold leakage current is investigated by MEDICI device simulation.

1 Introduction

The shrinking MOSFET has an increasing subthreshold leakage current caused by various mechanisms. For example, the band-to-band tunneling (BTBT) current from drain to channel results in a large subthreshold leakage current in a 50nm MOSFET [1]. Recently, the double-gate (DG) fully depleted (FD) MOS was investigated. In the DG-MOS, the channel region is intrinsic or lightly doped silicon so that the threshold voltage fluctuation problem can be avoided. The reduced leakage current has been proven [2]. In this paper, a DG-NMOS structure shown in Fig. 1 is simulated using MEDICI device simulator. The transfer characteristics of the DG-NMOS with the different gate material work functions ϕ_m are shown in Fig. 2. It can be seen that the threshold voltage can be adjusted by the work function of the gate material. However, the band-to-band tunneling leakage still exists in this DG-NMOS, when the transistor is turned off. As shown in Fig. 1, the band-to-band tunneling is still on, when $V_{gs} = 0V$. Fig. 3 shows the band diagram of this off-state DG-NMOS. The bending of bands enables the band-to-band tunneling at the junction of channel-drain. It seems that with the scaling dimension of MOSFET, the increasing leakage current is always a problem because of the n-p-n or p-n-p structure of MOSFET.

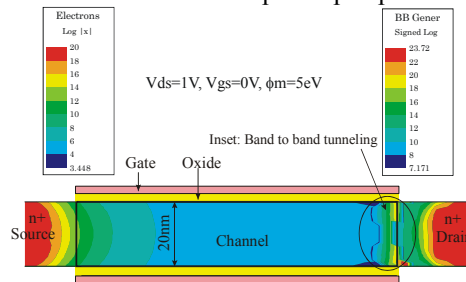


Fig. 1 NMOS structure and contour of the band-to-band tunneling generation rate and the electron density in an off-state DG-NMOS, $V_{ds}=1V$, $V_{gs}=0V$.

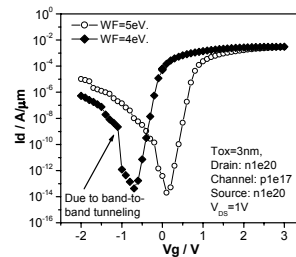


Fig. 2 Transfer characteristics of DG-NMOS with different gate materials, $\phi_m = 4$ or 5 eV.

2 Simulation of double-gate TFET

The structure of the simulated tunneling transistor in this work is a MOS-gated reverse-biased p-i-n diode. Considering the high barrier of the reverse-biased p-i-n junction, the leakage current of TFET will be very low.

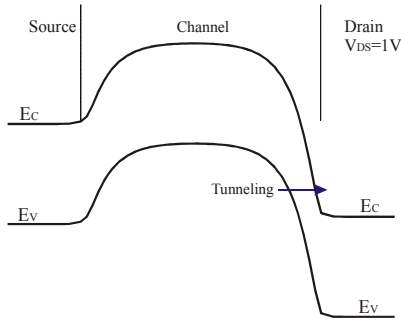


Fig. 3 Band diagram of a off-state DG-NMOS with $\phi_m=5\text{eV}$. ($V_{ds}=1\text{V}$ and $V_{gs}=0\text{V}$)

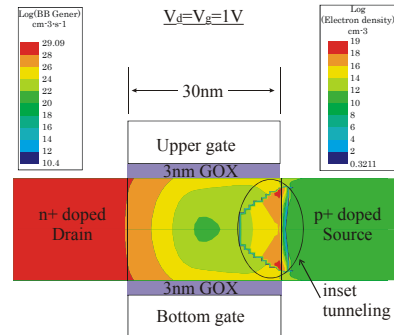


Fig. 4 Simulated DG-TFET structure and the contours of band-to-band tunneling generation rate and electron density in this TFET.

2.1 Subthreshold leakage of TFET

A double-gate TFET is simulated and the details of the simulated structure are shown in Fig. 4. The working principle of TFET is illustrated in the band diagram shown in Fig. 5 (the positive V_g can reduce the tunneling barrier). The simulated transfer I - V characteristics of this double-gate TFET with the BTBT model turned on are shown in Fig. 6. The minimum leakage current of 30nm TFET can be reduced to $1 \times 10^{-16} \text{A}/\mu\text{m}$ at 1.0 V supply voltage, as can be explained by the band diagram of the off-state TFET (Fig. 5). At $V_{ds}=V_{gs}=1\text{V}$, the band-to-band tunneling generation rate and the electron density are plotted in Fig. 4. The subthreshold leakage current of TFETs with various channel lengths is investigated. The transfer characteristics of DG-TFETs with various channel lengths are shown in Fig. 7. The double-gate TFET with 20nm channel length still has much larger current gain and lower subthreshold leakage than the projected 25nm high performance NMOS in the ITRS roadmap 2003.

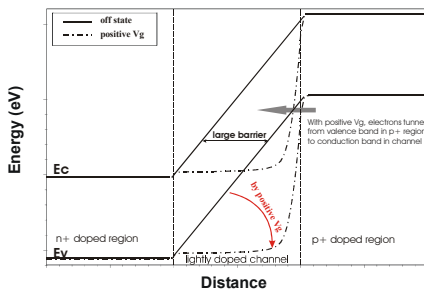


Fig. 5 Band diagram of a MEDICI simulated band diagram of the TFET.

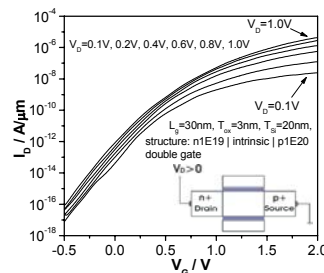


Fig. 6 Transfer characteristics of the double-gate TFET with V_{ds} as differing parameters.

2.2 Drain current saturation in TFET

Following the simulation results mentioned in [3], the high performance TFET was fabricated. It is found by measurements that the drain current saturation behavior of TFET is better than that of MOSFET. Fig. 8 shows the linear plot of experimental TFET output characteristics. A series of band diagrams of the simulated device are studied. The effect similar to the pinch-off effect in MOSFET where the pinch-off starts when $V_{gs} - V_t = V_{ds}$ is observed. Fig. 9 shows the electron density in a TFET with $V_{ds} = 3V$ and $V_{gs} = 2V$. The channel at the drain-channel junction is pinched off. When the pinch-off starts, the increase of the drain potential cannot change the voltage-drop at the tunneling junction which is at the channel-source junction and the drain current is saturated. Comparing the conductivity of MOS channel to the tunneling junction in TFET, it is obvious that the tunneling junction has a higher resistance and is the bottleneck of the drain current. Therefore, although the saturation of the drain current in TFET is caused by the pinch-off of the MOS channel, the saturated current density is determined by the tunneling effect. For this reason, the channel length modulation in the pinch-off effect has only a very small effect on the drain current of TFET. Thus, the drain current saturation behavior of TFET can be better than that of MOSFET.

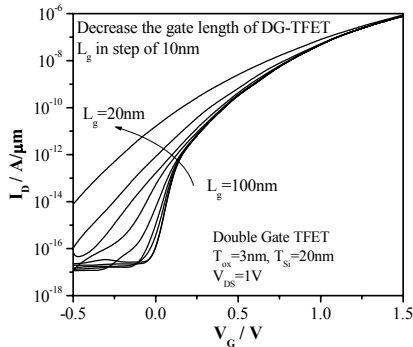


Fig. 7 Transfer characteristics of the double-gate TFETs with various channel lengths, $t_{ox} = 3nm$ and $t_{si} = 20nm$.

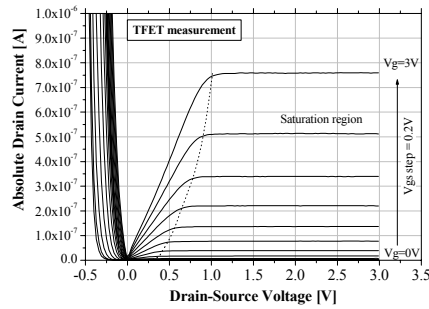


Fig. 8 Linear plot of the experimental TFET output characteristics.

2.3 Hot electrons in TFET

TFET is also a hot electron device where the electrons are injected into the channel region through the tunneling barrier. Due to the short and intrinsic channel, ballistic electron transport can be realized in TFET, when its channel length is reduced below 30nm. Fig. 10 shows the band diagram of the on-state TFET. The distribution of electrons energy in the p^+ doped region is non-Maxwellian. The average energy of the injected electrons depends on V_{ds} . The portion of the ballistic transport will increase with the increasing V_{ds} . An interesting phenomenon is that the tunneling barrier in TFET is also an energy filter of hot electrons. For the electrons in the p^+ region with lower energy, the barrier becomes wider for them to tunnel through. That means only

a portion of electrons with the energy close to the Fermi-level in p^+ region can tunnel through the tunneling junction and inject into channel. The overshoot of electron velocity due to the high tunnel injection energy was found in the simulation. The velocity overshoot is independent of the channel doping concentration. Near the n^+ drain where the electron density becomes higher the electron velocity decreases rapidly. Similar to bipolar device, the operating speed of TFET is determined by the transit time through the channel region and the product of parasitic capacitance and source/drain resistance. In TFET, both source and drain are heavily doped, the device operating speed can be improved for the short electron transit time through channel.

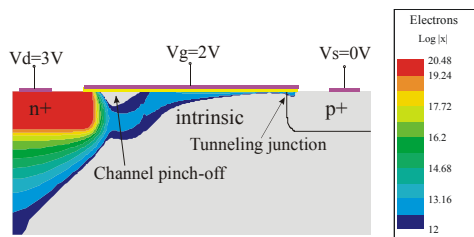


Fig. 9 Pinch-off of the channel in a TFET.

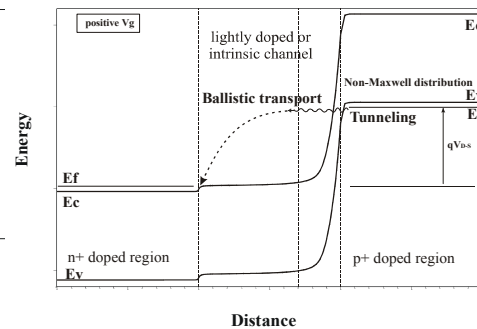


Fig. 10 Band diagram of on-state TFET. The hot electron injection is shown. The ballistic transport in channel is possible.

3 Conclusion

Simulations show that TFET has the advantages of low subthreshold leakage, better drain current saturation, and shorter transit time through channel region than MOSFET. Our additional simulations on subthreshold swing of TFET also show that the subthreshold swing of TFET is not limited by kT/q because of the tunneling effects.

Acknowledgements

This work is supported by the Deutsche Forschungsgemeinschaft (DFG).

Reference

- [1] T. Schulz, W. Rösner, L. Risch, and U. Langmann, "50-nm vertical sidewall transistors with high channel doping concentrations", IEDM Tech. Dig., pp. 61-64, 2000.
- [2] Y.-K. Choi, T.-J. King, and Ch. Hu, "Spacer FinFET: nanoscale double-gate CMOS technology for the terabit era", Solid-State Electronics, vol. 46, pp. 1595-1601, 2002.
- [3] P.-F. Wang, Th. Nirschl, D. Schmitt-Landsiedel, and W. Hansch, "Simulation of the Esaki-tunneling FET", Solid-State Electronics, vol. 47, pp. 1187-1192, 2003.