An Analysis of the Effect of Surrounding Gate Structure on Soft Error Immuniy

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Abstract

This paper clarifies the effect of surrounding gate structure on soft error immunity in floating body type devices. Alpha-particle-induced soft error simulations were performed with surrounding gate, tri-gate and double gate transistors as transfer devices of DRAM cells. In case of surrounding gate transistor (SGT) cell, the loss of the stored charge in the storage node after an alpha-particle strike can be drastically reduced because the surrounding gate structure can suppress the floating body effect most efficiently by the highest controllability of the body potential compared with other gate structures. Therefore, SGT DRAM cell is a promising candidate for future high density DRAMs having high soft error immunity.

1 Introduction

In order to realize future high density DRAMs, three dimensional (3-D) structured SGT DRAM cell has been proposed [1]. The bird's-eye view of floating channel type surrounding gate transistor (FC-SGT) DRAM cell and its equivalent circuit are shown in Fig. 1(a) and (b), respectively. One cell itself arranges an FC-SGT and a 3-D storage capacitor in a silicon pillar vertically and achieves cell area of $4F^2$ per bit. On the other hand, soft errors in high density DRAMs become serious concerns as device structures are scaled sown, and DRAM designs require also high soft error immunity. It has been reported that the surrounding gate structure can suppress the floating body effect more efficiently compared with planer SOI MOS structure [2]. This paper clarifies the effect of surrounding gate structure on soft error immunity by comparing three floating body devices with 3-D gate structures: SGT, tri-gate [3] and vertical double gate transistor cells.

2 Soft Errors in FC-SGT DRAM Cell

Physical models of soft errors in a FC-SGT DRAM cell are shown in Fig. 2. When an alpha particle penetrates the silicon pillar, electron-hole pairs are generated inside the cell as shown in Fig. 2(a). After the strike, generated electrons are collected to the storage node or bit lin (BL) due to the funneling [4] and diffusion mechanisms. Holes are accumulated in the body region. Therefore, the body potential is raised by the floating body effect. In a "0" state, the storage node junction is forward-biased. The parasitic bipolar effect occurs in the emitter (storage node)-base (body)-collector (BL)

structure. Electrons are transferred from the storage node to BL as shown in Fig. 2(b). This parasitic bipolar current leads to the loss of the stored charge in the storage capacitor. The parasitic bipolar effect can occur in other floating body devices as well as in FC-SGT. Therefore, the floating body effect must be suppressed to improve the soft error immunity of floating body devices.

3 Results and Discussion

The soft errors under the "0" condition shown in Fig. 2(b) were simulated by using 3-D device simulator [5], where V_{DD}=1.5 V. For simplicity, only the transfer devices were considered. Fig. 3 shows the conditions of 3-D device simulation for three floating body devices with different gate structures: SGT, tri-gate, and double gate cells. Gate, source and drain correspond to word line (WL), storage node and BL, respectively. Fig. 3(d) shows cross-sectional view along (A1)-(A2) of these cells and the alpha particle track. Device parameters are listed in Table 1. Under these conditions, the volume of silicon region and hence the total number of electron-hole pairs generated inside a cell are the same for these three cells. In addition, the gate work function is set so as to satisfy the same leakage current comparable to 0.88 fA/cell [6] for each device. Therefore, it is possible to analyze only the effect of gate structure on the floating body effect by investigating the parasitic bipolar current.

Fig. 4 indicates the potential profiles along the alpha particle track at 0 and 100 ps in three cells with different gate structures. The rise of the body potential due to the floating body effect is most effectively suppressed by SGT cell. At 100 ps, the potential barrier V_1 for SGT cell is higher than V_2 for tri-gate or V_3 for double gate cell. Transient source current characteristics after the strike for each cell are shown in Fig. 5(a). In Phase I, the generated electrons are collected into source or drain due to the funneling and diffusion mechanisms. In Phase II, the parasitic bipolar effect occurs. Electrons are transferred from source to drain, so that the source current changes from the electron collection mode to the ejection mode. The parasitic bipolar current is decreased gradually because the accumulated holes in the body region are decreased due to the recombination process and the body potential is recovered. After 500 ms, the constant leakage current flows. The parasitic bipolar current in SGT cell is the smallest. Fig. 5(b) shows transient ejected charge characteristics at source electrode. In a "0" state, source charge ejection means the loss of the stored charge. The source ejected charge in SGT cell is the smallest due to the smallest parasitic bipolar current compared the other cells. The source ejected charge until 1 s is decreased to 44% of tri-gate or 15% of double gate cell. This result shows that SGT cell has higher soft error immunity compared with the other cells.

4 Conclusions

This paper clarifies the effect of surrounding gate structure on soft error immunity in floating body devices. In case of SGT cell, the surrounding gate structure can suppress the floating body effect most efficiently. As a result, the loss of the stored charge can be decreased to 44% of tri-gate or 15% of double gate cell. Therefore, SGT cell is a promising candidate for future high density DRAMs having high soft error immunity.

References

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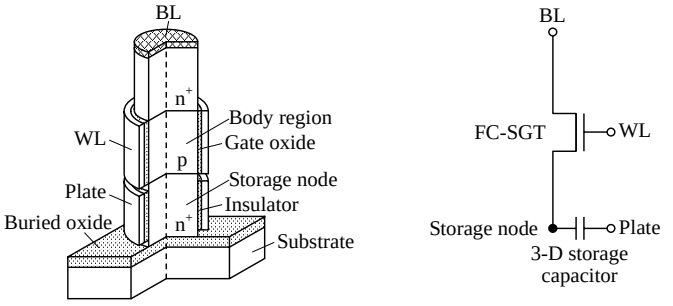
[5] ATLAS ver. 5.6.0.R, Silvaco int.
[6] International Technology Roadmap for Semiconductors 2001 Edition.

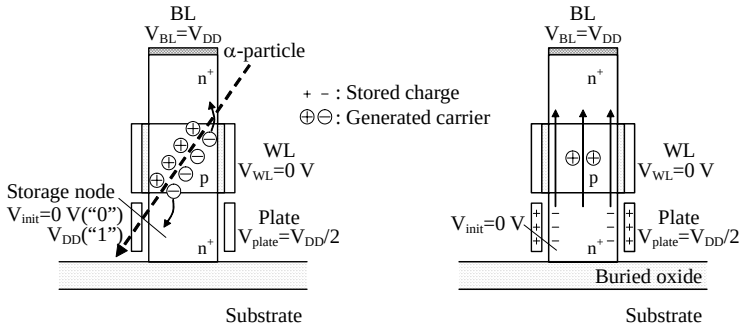
Parameter	**Meaning**	**Value**
L	Gate length	200 nm
T_{OX}	Gate oxide thickness	3.6 nm
T_{Si}	Silicon film thickness	90 nm
W	Silicon film width	90 nm
N_D	Impurity concentration of diffusion layers	10^{20} cm^{-3}
N_A	Impurity concentration of body region	10^{17} cm^{-3}

Table 1: Device parameters.



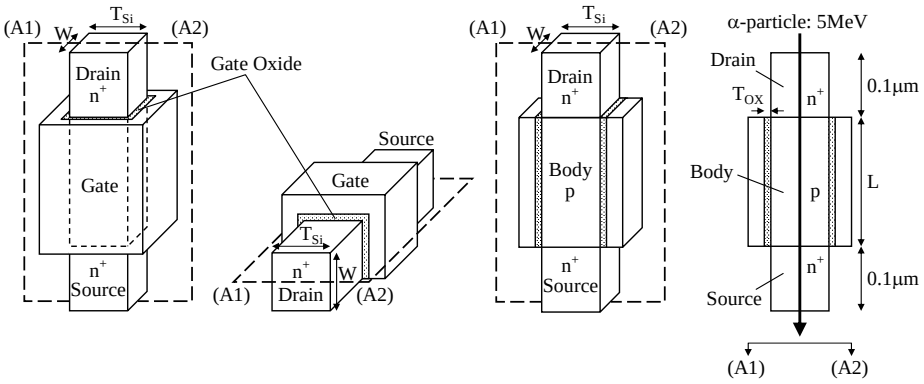
(a) (b)

Figure 1: (a)Bird's-eye view. (b)Equivalent circuit of FC-SGT DRAM cell.



(a) (b)

Figure 2: Physical models of soft errors in FC-SGT DRAM cell. (a)Electron collection to the storage node or BL. (b)Parasitic bipolar current in a "0" state.



(a) (b) (c) (d)

Figure 3: Simulation conditions for (a)SGT, (b)tri-gate and (c)double gate cells. (d)Cross-sectional view along (A1)-(A2) of these cells.

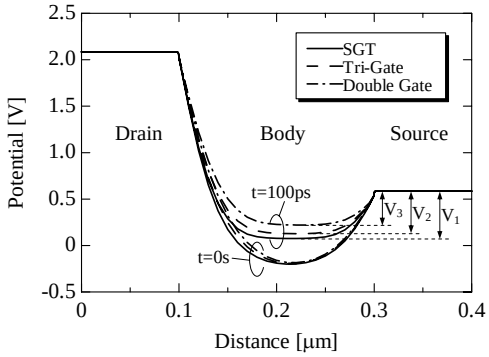
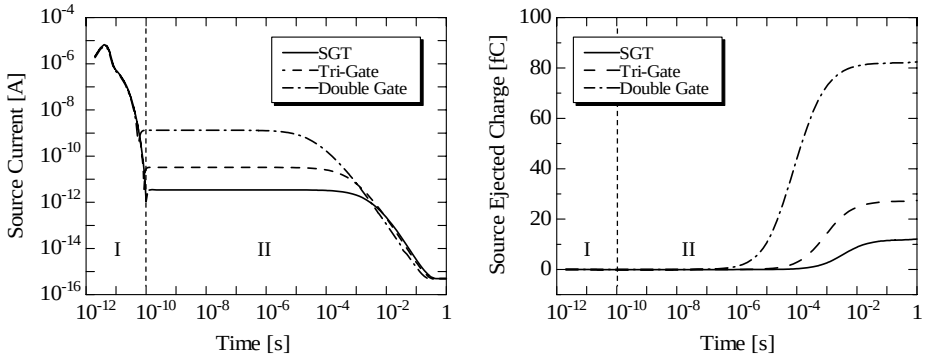


Figure 4: Potential profiles in floating body devices with different gate structures.



(a) (b)

Figure 5: (a)Source current and (b)source ejected charge characteristics as a function of time in floating body devices with different gate structures.