Simulation of Nanofloating Gate Memory with High-k Stacked Dielectrics

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***Abstract*— Scaling of conventional floating gate non-volatile memory cells towards the nanometer range is jeopardized by the lack of scalability of the tunnel oxide. In this paper, we discuss the advantages of using high-k materials for nanofloating gate memory structures by means of numerical device simulations.**

I. Introduction

The unscalability of the tunnel oxide of the Flash memory cells imposes high voltages for triggering the tunneling operation. Moreover, the channel length cannot be scaled down due to the aggravation of the short channel effects [1]. Recently, high-k materials [2] have been suggested as alternative tunnel dielectrics [3] and new tunnel barrier concepts have been proposed [4], [5]. These were shown to have potential for low-voltage low-power operation and a good chance for integration in a mainstream CMOS technology.

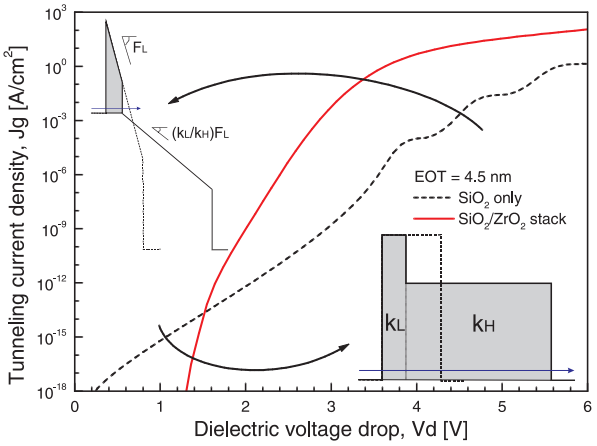

Fig. 1. Surface potential versus applied bias calculated with the simplified method (lines) and self consistent results (symbols). This excellent agreement has been checked for different oxide thicknesses and substrate dopings.

II. Principle and Device Structures

An asymmetric VARiable Oxide Thickness (VARIOT) stack consists of two dielectric layers, one of which is a high-k dielectric, the other being a material with a low dielectric constant and may conventionally be considered SiO_2. Due to the difference in the dielectric constant of the two dielectric layers of the stack, when a voltage drops over the stack the electric field redistributes as compared to the case of a single dielectric layer, being significantly higher in the SiO_2 layer [4]. Consequently, a VARIOT stack allows for high tunneling currents at moderate voltage drops across the stack, and has a steep slope of the current-voltage characteristic at low voltages, due to its large physical thickness. It is therefore an ideal candidate for replacing the tunnel oxide in a stacked gate memory cell, as it allows lowering the programming voltage, or equivalently, reducing the programming time at the same programming voltage. Moreover, the electrical thickness may be reduced, enabling to effectively scale down the transistor channel.

The asymmetric VARIOT stack is an unidirectional tunnel dielectric. To enable similar tunneling properties in the opposite direction, a symmetric VARIOT stack should be used. It consists of three dielectric layers, with the high-k dielectric being sandwiched between two low-k (i.e. SiO_2) layers. We demonstrate these unique properties of the VARIOT tunnel dielectric by simulating [6] two stacked gate structures with an either asymmetric (Fig. 2, left) or symmetric (Fig. 2, right) VARIOT stacks.

III. Results and Discussion

Floating gate transistor structures with a channel length of about 50 nm were considered. The doping levels were adjusted so as to yield a threshold voltage

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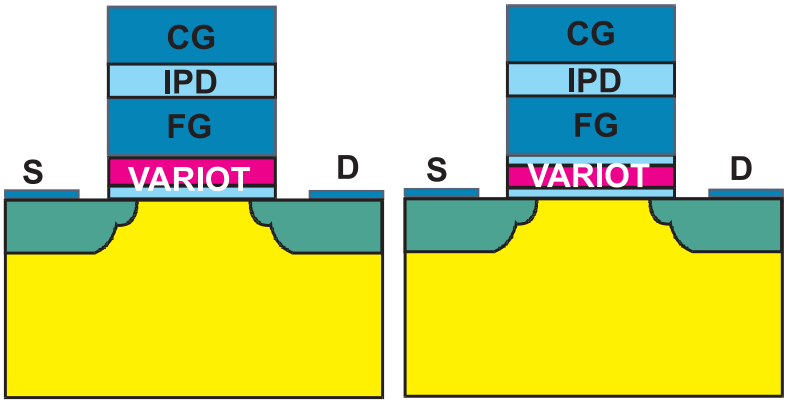

Fig. 2. Schematic drawing of a stacked gate structure with an asymmetric (left) and symmetric (right) VARIOT tunnel dielectric stack between the floating gate (FG) and the channel.

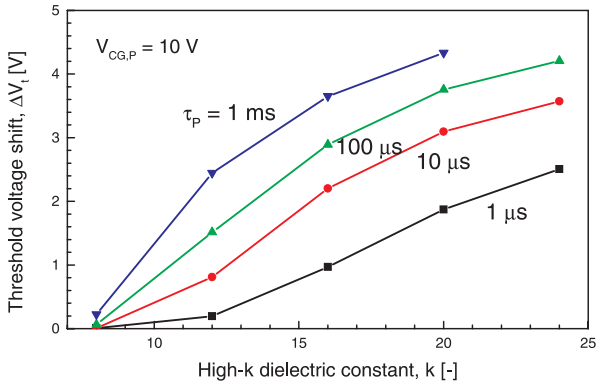

Fig. 3. Influence of the dielectric constant on the threshold voltage shift when using a VARIOT stack as a tunnel dielectric. The stack is 2 nm SiO_2 and 10 nm high-k material, with an assumed barrier height of 2 eV.

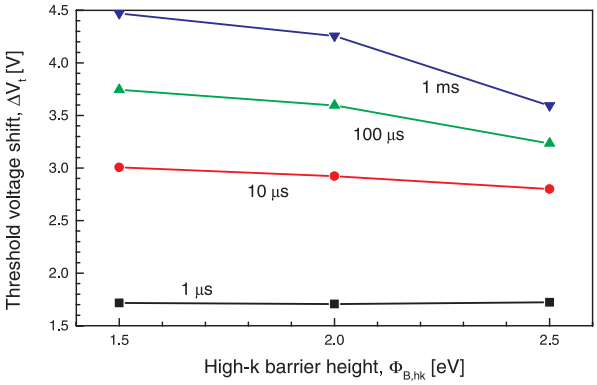

Fig. 4. Influence of the barrier height of the high-k material on the threshold voltage shift when using a VARIOT stack as a tunnel dielectric. The stack is 2 nm SiO_2 and 10 nm high-k material, with an assumed dielectric constant of 20.

of the contacted floating gate structure of around 1 V, and the poly-poly coupling capacitance was adjusted so as to have a ratio $V_{FG}/V_{CG} \approx 0.65$ for a virgin device. Programming the floating gate device is realized by applying a positive pulse on the control gate (CG), with all the other contacts grounded, whereas the erase is done by applying a negative pulse on the CG.

A. Impact of high-k material parameters

The impact of the dielectric constant of the high-k material in a VARIOT stack is shown in Fig. 3, where stacks of 2 nm SiO_2 and 10 nm high-k thickness have been considered. The barrier height of the high-k material has been fixed to 2.0 eV. The threshold voltage shift increases with the high-k dielectric constant, at any value of the programming time.

It has to be noticed that by increasing the dielectric constant in the stack, the electrical thickness decreases. Therefore, to maintain the coupling of the cell, additional coupling capacitance has to be provided. The conventional way to solve this issue is to extend the coupling area between the floating gate and the control gate. This was also adopted in this work, where the interpoly dielectric thickness is fixed at a constant value. However, this solution conflicts with the requirement of reducing the cell area, and an alternative method would be to make use of high-k materials as interpoly dielectrics [7], allowing to significantly scale down their effective thickness and maintain a good coupling without significant penalties with regard to the cell area.

The barrier height of the high-k material influences the programming performance of the VARIOT stack as

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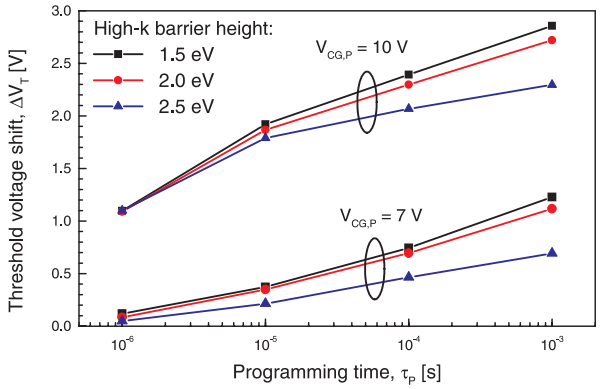

Fig. 5. The threshold voltage shift versus programming time, for different high-k barrier heights for an asymmetric VARIOT stack with 2 nm SiO_2 and 10 nm high-k dielectric, at different programming voltages. The high-k dielectric constant is fixed at 20.

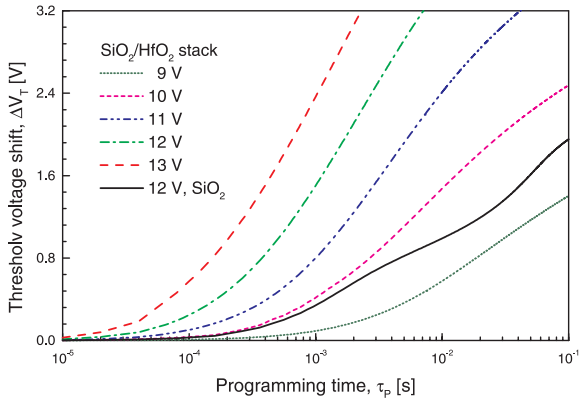

Fig. 6. Programming transients for an asymmetric VARIOT stack at different control gate voltages. The transient corresponding to a SiO_2 of identical electrical thickness is shown for comparison. The initial V_T corresponds to an electrically neutral floating gate.

well. Fig. 4 shows the V_T shift for a stack of the same physical thickness and a high-k dielectric constant fixed at 20, programmed at 10 V on the CG. A lower high-k barrier height is more effective in achieving large V_T shifts in short programming times, although this might be detrimental to retention. However, as compared to the effect of the high-k dielectric constant, the threshold voltage shift is less sensitive to variations of the high-k barrier height. Moreover, the effect of the barrier height on the V_T shift depends on the programming voltage as well (Fig. 5): increasing the programming voltage reduces the effect of the high-k barrier height, the shorter the programming time, the more so. This is due to the fact that at high-enough biases the effective tunneling barrier is nearly identical, being given by the SiO_2 layer only, at least in the beginning of the programming pulse.

B. Al_2O_3 and HfO_2 VARIOT stacks

Threshold voltage shift during programming operation is shown in Fig. 6, for several programming voltages. For the sake of simplicity, stacks of 7 nm EOT have been considered, although the real benefit of the VARIOT stack is in a thickness range of less than 5-6 nm EOT, where a single SiO_2 layer cannot guarantee 10 years of retention, even in a theoretical situation. For comparison, a transient of conventional SiO_2 tunnel dielectric obtained with identical simulation conditions is shown.

At least 2 V decrease in the program voltage is possible for stacks with HfO_2, and up to 1.5 V for stacks with Al_2O_3 (Fig. 4) at identical program times, as compared to a single SiO_2 layer of identical electrical thickness (EOT). Equivalently, programming at a given voltage results in significant decrease of the programming time, i.e. about 50 times faster at 12 V, for the case illustrated in Fig. 7 (HfO_2 stacks). At very high programming voltages, the programming time tends to be the same, for SiO_2 and VARIOT stacks. This situation corresponds to biases for which the electric field in the SiO_2 layer is high enough so that the tunneling barrier becomes identical for both conventional SiO_2 and VARIOT tunneling dielectrics. Hence, the electrically identical VARIOT stack delivers maximum performance in the regime corresponding to direct tunneling through only the thin SiO_2 layer of the stack.

Unfortunately, the asymmetric stacks are not very effective in erasing at such large physical thickness. Erasing through asymmetric layers becomes possible for ultrathin VARIOT stacks only. An erase time in the order of 1 s was estimated, as checked for Al_2O_3 stacks with EOT's of 4 to 5 nm, and with erase voltages $V_{CG,E}$ between -7.5 V and -10 V. Although orders of magnitude slower than the programming time, this may be accepted given the block chacarter of the erase operation in Flash memory arrays.

To improve the eraseability through VARIOT stacks, a symmetric version in which bidirectional tunneling is possible at comparable speeds is a potential solution. Fig. 8 shows programming curves for symmetric stacks of 5.6 nm EOT, with a SiO_2 of 1.8 nm. Erasing in a time of around 1 ms or less, with a V_T shift of 2.5 V is achievable at ± 10 to ± 12 V when using HfO_2 as high-k dielectric. We expect that stacks with e.g. ZrO_2 would show similar performance, as can be deduced from Figs. 3,4. Compared with today's average voltage of tunneling based Flash cells [8] of ± 15 to

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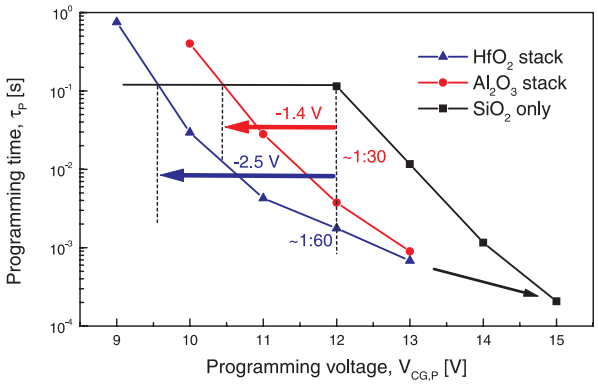

Fig. 7. Programming time as a function of program voltage required to achieve a V_T shift of 2 V as compared to the virgin V_T for asymmetric VARIOT stacks with HfO_2 and Al_2O_3. Eventually, at very high programming biases the programming speed through the VARIOT stack approaches that of the SiO_2 layer.

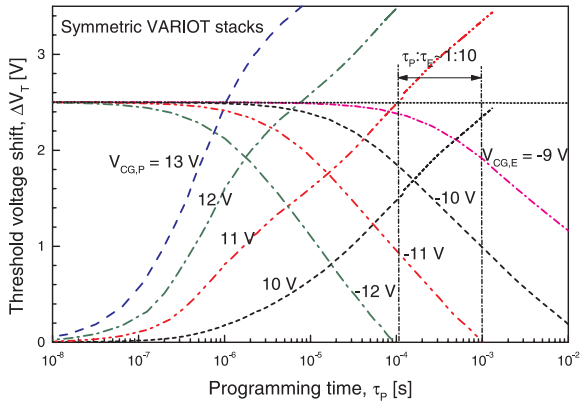

Fig. 8. Transient characteristics corresponding to the program/erase operations for symmetric stacks of 5.6 nm EOT.

± 17 V, it can be concluded that VARIOT stacks have a high potential for lowering the operating voltages of the floating gate structures. The VARIOT barrier has a much larger physical thickness than a SiO_2 tunnel dielectric of similar electrical thickness, which has a beneficial impact on retention, at low bias (e.g. under read-out conditions). Moreover, the reduced electrical thickness improves the short channel effect [1], allowing further downscaling.

The performance of the symmetric VARIOT stack can be tuned by changing the thickness of the oxide layer. A decrease of the thickness of only 5 Å yields an over 1 order of magnitude improvement of the program/erase times variation (Fig. 9). Eventually, the outer layer thicknesses may be optimized separately, for program and erase operations, respectively.

In this paper we only addressed the advantages of

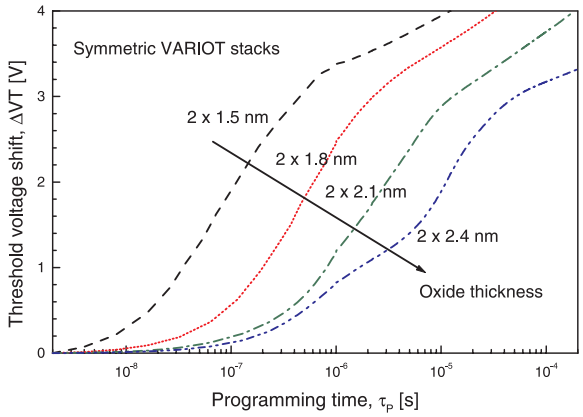

Fig. 9. Threshold voltage shift for symmetric VARIOT stacks. The interfacial oxide thickness plays a crucial role in the performance of the stack.

using a VARIOT stack when replacing the tunnel oxide for program or both program/erase operations in a stacked gate cell. We expect VARIOT stacks to also offer significant decrease of the operating voltages when used as an unidirectional tunnel dielectric for erasing devices programmed by hot carrier injection.

IV. Conclusion

Device simulations showed that a considerable decrease of the program/erase voltages combined with short program/erase times is possible when using SiO_2/high-k dielectric stacks. Preliminary experimental results [9] confirmed this conclusion. The larger physical thickness of the stack provides sufficient retention whereas the reduced electrical thickness allows to further scale down the channel length.

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