Effects of Gate-to-Body Tunneling Current on PD/SOI CMOS Latches

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***Abstract*— This paper presents a detailed study on the effect of gate-to-body tunneling current on PD/SOI CMOS latches. The physical mechanism and its impact on the initial quiescent states and performance of the latches are analyzed. It is shown that the effect on latch setup time is particularly significant due to the compounding effect of the master-slave configuration.**

I. Introduction

Recently, the gate-to-body tunneling current (I_{gb}) in PD/SOI device resulting from the electron tunneling from the valence band (EVB) [1] has been shown to charge/discharge the floating-body, thus changing the body voltage and V_T and affecting circuit operations [2, 3, 4, 5]. In this paper, we present a detailed study on the effect of gate-to-body tunneling current on PD/SOI CMOS latches in a 1.2 V, 0.13 μm PD/SOI technology with L_{poly}= 0.075 μm, physical t_{OX} = 1.5 nm, t_{Si} = 120 nm, and t_{BOX} = 145 nm. Various operating modes of latches are examined. It is shown that the effect can compound in master-slave configuration, causing significant degradation in the latch setup time.

II. Clock-Rise to Latch Node Delay

Fig. 1(a) shows the schematic of an unbuffered CMOS latch [6]. The latch is assumed to be in an initial quiescent state with input at "Low", the DOUT node conditioned to "Low", and the clock signal C1T at "Low". The body voltages of pass-transistor Q1N and Q1P will be at "Low" (Ground). Thus, there is zero bias across the gate and body of Q1N, hence no gate-to-body tunneling current into or out-of the body of Q1N. On the other hand, since C1C is at V_{DD}, there is full V_{DD} across the gate and body of Q1P, resulting in EVB from its body to the gate. This gate-to-body tunneling current charges the body, thus increasing V_T and making Q1P "weaker". For the nMOS in the forward inverter (Q2N), with DOUT at "Low", its body sits at a diode cut-in voltage determined primarily by the balance of the back to back drain-to-body and body-to-source junctions. Thus, there is a "small" negative bias across the gate and body, resulting in "small" EVB from the gate to the body. This "small" body-to-gate tunneling current discharges the body, thus increasing V_T slightly and making Q2N "slightly weaker". For the pMOS Q2P, with V (G, S, D) = (0, V_{DD}, V_{DD}), its body sits at V_{DD}. Hence, there is a "large" negative bias across the gate and body, resulting in EVB from the gate to the body. This body-to-gate tunneling current discharges the body, thus decreasing V_T and making Q2P "stronger" [4, 5]. The changes in the strength of Q3N, Q3P, Q4N, and Q4P are deduced in the same way and shown in Fig. 1(a).

Fig. 1(b) depicts the timing diagram for the case where the clock signal C1T goes to "High" and then switches continuously at 500 MHz with 50% duty cycle. The input signal IN is set up before the clock-rising transition. After "writing" the latch, the input returns to "Low" and remains "Low" through the next cycle. So, in the odd clock cycles, the input IN writes "0" into the latch node L1 (complement of IN), whereas in every even clock cycle, the input IN writes "1" back into the latch node L1 (complement of IN). Both clock and input signal have a slew of 100 ps. The output load COUT is 50 fF.

Fig. 2(a) shows the percent change in the clock-rise to L1-fall delay due to the gate-to-body tunneling current as functions of time for the initially "Low" condition. The percentage change in the delay is defined as [(Delay without I_{gb}) - (Delay with I_{gb})]/(Delay without I_{gb}) x 100%. Notice that the latch delay is determined predominantly by the forward path, since once C1T rises,the transmission gate (Q4N/Q4P) in the feedback path shuts off, thus completely isolating the feedback inverter. This transition (input IN "High" to write "0" into latch node L1) is dictated by the pass transistors Q1N/Q1P and Q2N. For this case, (a) the strength of Q1N is not affected, while Q1P is "weaker", and (b) Q2N is "slightly weaker", hence slower in pulling-down node L1. Thus, both elements cause "slow-down" of the circuit. The effect is more pronounced at lowered temperature since I_{gb} has a much weaker temperature dependence compared with other body charging/discharging current components [4]. At 25 ^{o}C, the slow-down is 3.1% initially and 1.1% at t = 10000 ns.

Fig. 2(b) shows the case for the clock-rise to L1-rise delay (input IN "Low" to write "1" into latch node L1). This transition is dictated by Q1N ("no effect")/Q1P ("weaker") and Q2P ("stronger"). The speed-up due to the "stronger" Q2P is mostly offset by the slow-down due to the "weaker" Q1P in passing the "Low" state. Thus, overall speed-up is not significant (0.64% initially and 0.12% at t = 10000 ns at 25 ^{o}C).

Fig. 3(a) and 3(b) depict the situation for the latch in an initial quiescent state with input at "High" and the DOUT node conditioned to "High" The clock-rise to L1-fall delay is dictated by Q1N ("weaker")/Q1P ("no effect") and Q2N ("stronger"). The "weaker" Q1N significantly slows down the passing of a "High" state through the pass-gate, thus offsets most of the speed-up due to the "stronger" Q2N. Hence, the overall speed-up is not significant as shown in Fig 4(a) ($<$ 1.0% for all temperatures).

The case for the clock-rise to L1-rise delay under the initially "High" condition is shown in Fig. 4(b). As both elements (Q1N ("weaker")/Q1P ("no effect") and Q2P ("slightly weaker")) cause "slow-down" of the circuit, the delay change due to I_{gb} is more significant. At 25 ^{o}C, the slow-down is 6.8% initially and 0.3% at t = 10000 ns.

III. Transparent Mode

In "Transparent" mode, the forward transmission gate remains "open", and the input data simply flushes through. Fig. 5(a) depicts a latch under "Transparent" mode with input initially at "Low". The timing diagrams under study are shown in Fig. 5(b), where the clock signal C1T remains "High" and the input IN switches continuously at 500 MHz with 50% duty cycle and 100 ps input slew. The input-rise to L1-fall dealy is dictated by Q1N ("stronger")/Q1P ("no effect") and Q2N ("slightly weaker"). The speed-up due to "stronger" Q1N is partially offset by the slow-down due to "slightly weaker" Q2N, and the delay change is insignificant ($<$ 2.0% for all temperatures, not shown).

For the input-fall to L1-rise delay under initially "Low" condition, the delay is dictated by Q1N ("stronger")/Q1P ("no effect") and Q2P ("stronger"). As both elements speed up the circuit, the delay change due to I_{gb} is more significant (Fig. 6). At 25 ^{o}C, the speed-up is 5.8% initially and 2.1% at t = 10000 ns.

Fig. 7(a) and 7(b) depicts the situation for the latch under "Transparent" mode with input initially at "High". For the input-rise to L1-fall delay (Fig. 8), both elements (Q1N ("no

effect")/Q1P ("stronger"), and Q2N ("stronger")) speed up the circuit, and the delay change due to I_{gb} is quite significant (Fig. 8(a)). At 25 ^{o}C, the speed-up is 6.4% initially and 0.7% at t = 10000 ns.

The input-fall to L1-rise delay is dictated by Q1N ("no effect")/Q1P ("stronger") and Q2P ("slightly weaker). The speed-up effect due to Q1P is offset by the slow-down due to Q2P, and the delay change is insignificant (< 1.0% for all temperatures, not shown).

IV. Latch Setup Time

Setup time is one of the most important parameters in determining the latch performance and overall chip timing. Fig. 9 depicts a pair of latches connected in master-slave configuration with C1T clocking the master latch and C1C clocking the slave latch. Also shown are the timing diagrams for the setup time under different initial conditions. The input data must arrive at least one setup time before the C1T falling edge to be properly latched. Noting that the effect of I_{gb} is most significant for first cycle after long time of quiescence, Fig. 10 shows the setup time vs temperature. At 25 ^{o}C, the presence of I_{gb} degrades the setup time by 20% (0.042 ns vs 0.035 ns) for the initially "High" condition, and by 12% (0.047 ns vs 0.042 ns) for the initially "Low" condition. The degradation is significantly larger than that for the single latch cases discussed in the previous two sections, and is caused by the compounding effect of the master-slave configuration. For the initially "High" case, the master latch is in the initially "High" condition (Fig. 3(a)) undergoing input "falling" transition. Its input-fall to L1-rise delay (dictated by Q1N ("weaker")/Q1P ("no effect") and Q2P ("slightly weaker")) slows down. Furthermore, the slave latch is in the initially "Low" condition (Fig. 1(a)) undergoing input "rising" transition, and its input-rise (L1-rise) to L2-fall delay (dictated by Q1N ("no effect")/Q1P ("weaker") and Q2N ("slightly weaker)) also slows down. Thus, the slow-down of both master and slave latch compound to cause significant degradation (lengthening) of the set-up time. Similar compounding effect is also present for the initially "Low" case to cause significant degradation in the setup time.

V. Conclusion

We have presented a detailed study on the effects of gate-to-body tunneling current on PD/SOI CMOS latch. The degradation in the latch setup time is shown to be particularly significant due to the compounding effect of master-slave configuration. The results clearly indicate that the effect has to be fully understood and carefully accounted for to ensure proper latch operations and chip timing.

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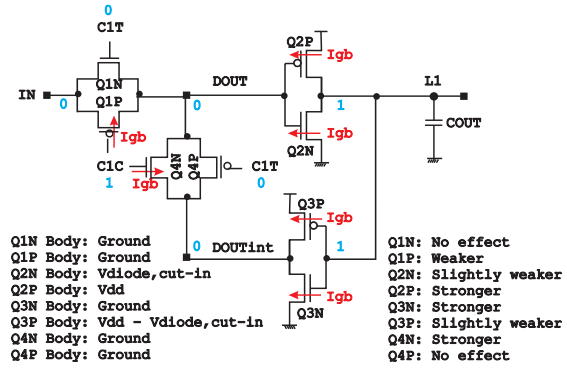
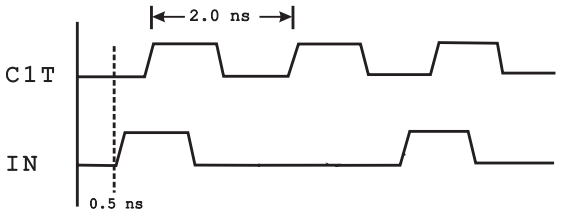
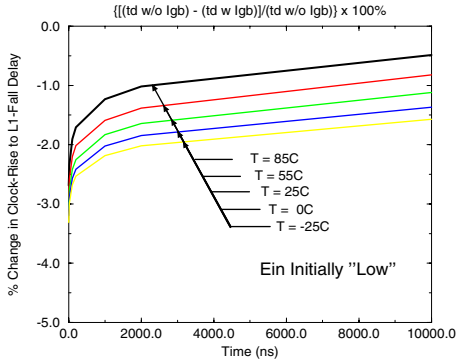


(a)

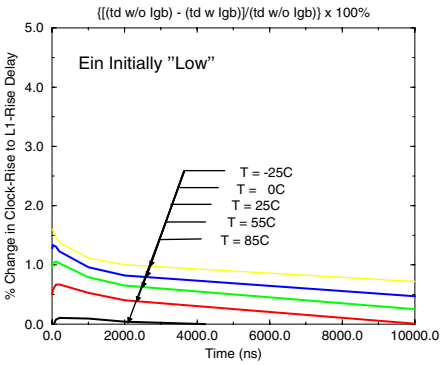


(b)

Fig. 1: (a) An unbuffered CMOS latch with a "trickle" inverter in feedback loop in an initial quiescent state with input at "Low", and (b) timing diagram for clock and input signal.



(a)



(b)

Fig. 2: Percent changes in (a) clock-rise to L1-fall delay, and (b) clock-rise to L1-rise delay due to I_{gb} under initially "Low" condition.

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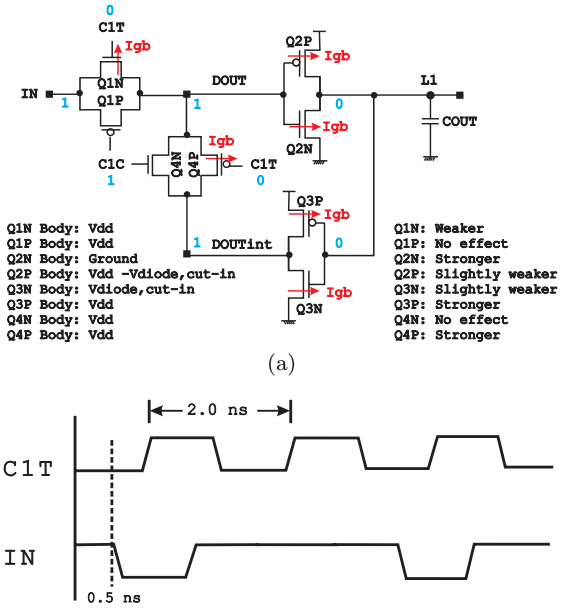
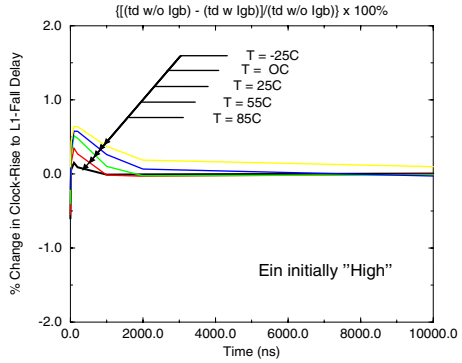


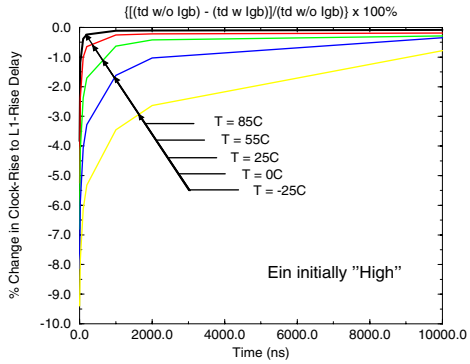
(a)

(b)

Fig. 3: (a) An unbuffered CMOS latch in an initial quiescent state with input at "High", and (b) timing diagram for clock and input signal.

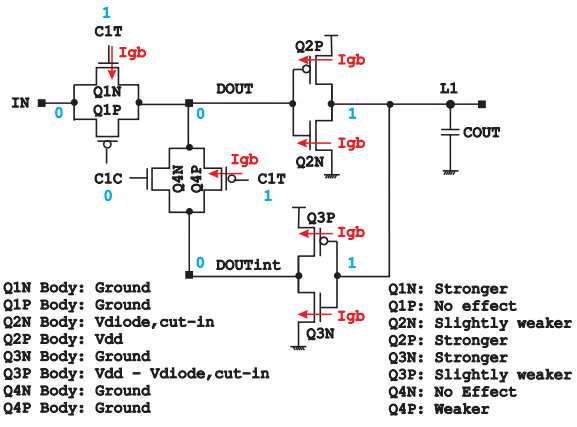


(a)

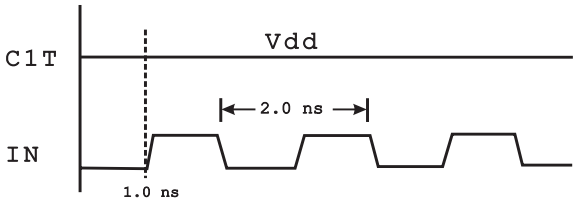


(b)

Fig. 4: Percent changes in (a) clock-rise to L1-fall delay, and (b) clock-rise to L1-rise delay due to I_{gb} under initially "High" condition.



(a)



(b)

Fig. 5: (a) An unbuffered CMOS latch under "Transparent" mode with input initially at "Low", and (b) timing diagram for clock and input signal.

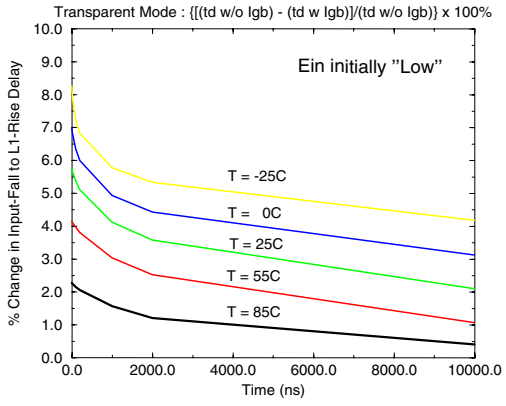


Fig. 6: Percent changes in input-fall to L1-rise delay due to I_{gb} under "Transparent" mode with input initially at "Low".

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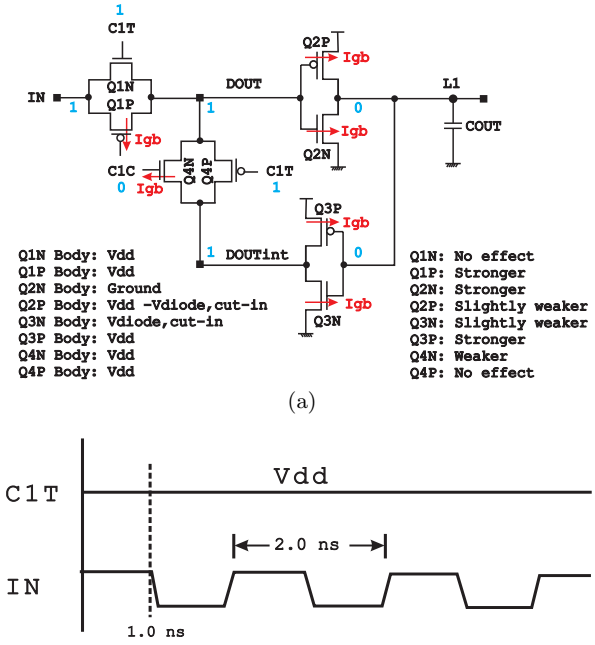

Fig. 7: (a) An unbuffered CMOS latch under "Transparent" mode with input initially at "High", and (b) timing diagram for clock and input signal.

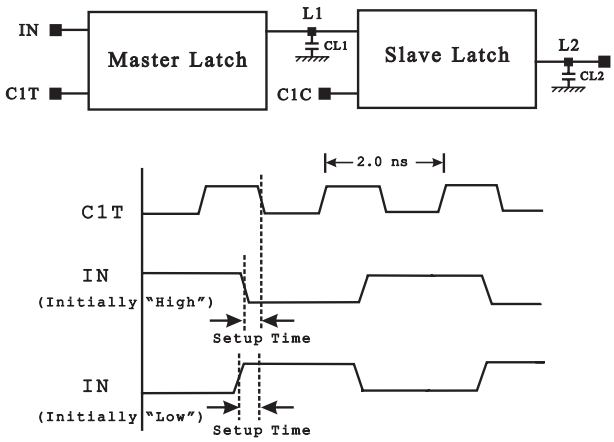

Fig. 9: A master-slave latch pair and timing diagrams for setup time.

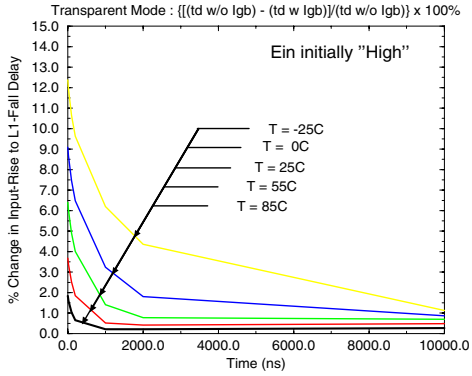

Fig. 8: Percent changes in input-rise to L1-fall delay due to I_{gb} under "Transparent" mode with input initially at "High".

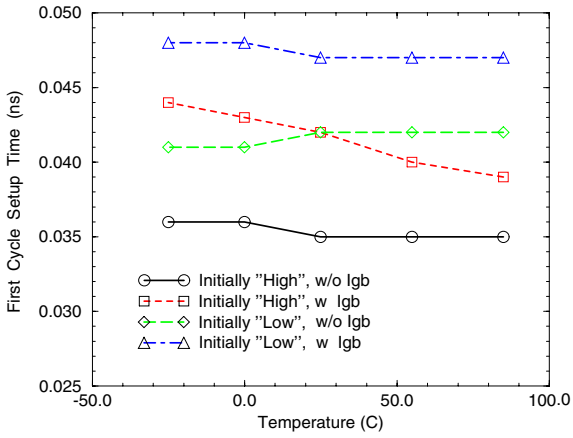

Fig. 10: First cycle setup time vs temperature for a master-slave latch pair.

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