An Investigation of the Electron Tunneling Leakage Current through Ultrathin Oxides/High-k Gate Stacks at Inversion Conditions

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***Abstract*— An efficient yet accurate model is used for investigating tunneling of minority carriers from the inversion layer of ultrathin MOSFET structures. The model is derived from the concept of the quasibound states lifetimes, which are calculated using a transfer matrix method based on Airy functions. Comparison with experimental data is provided. Performance of high-k materials is discussed and an investigation of their scalability for future CMOS technology nodes is carried out.**

I. Introduction

Continued CMOS technology downscaling requires ultrathin dielectric layers. Consequently, quantum-mechanical phenomena like gate leakage tunneling currents become increasingly important. Alternative solutions have to be found to maintain the gate leakage at an acceptable level [1]. To this goal, high-k gate dielectrics [2] were proposed, which, due to their increased dielectric constant allow for increased physical thickness at similar driving capability. However, their deposition often leads to the formation of an interfacial layer, thus diminishing their potential scalability. In this paper, we investigate the tunneling current through such stacked gate MOS structures biased in inversion and discuss the potential of several high-k materials for replacement of SiO_2 as gate dielectric from a gate leakage point of view for future low operating power (LOP) and low stand-by power (LSTP) technology nodes.

II. Modeling, Experimental Correlations and Simulations

The MOS potential and charge distributions are calculated using a six-valleys effective mass framework, yielding a surface potential consistent with the inversion charge density. The first three energy subband levels and the corresponding 2D charge densities of the lower energy (unprimmed ladder) and higher energy (primed ladder) valleys are taken into account [3]. The tunneling current originating from inversion layer carriers is calculated as the number of electrons decaying from the confining potential well into the gate electrode:

$$J_{2D,inv} = q \sum_{i,j} \frac{N_{ij}}{\tau(E_{ij})} \tag{1}$$

where the sum runs over each energy valley i and subband j. The lifetime $\tau(E_{ij})$ of the quasibound (QB) states are calculated using a semiclassical approach [4] and depends on the impact frequency f with which a QB particle hits the walls and on the probability $\mathcal{T}$ to escape the potential well by tunneling through the thin dielectric barrier:

$$\frac{1}{\tau(E_{ij})} = f(E_{ij}) \cdot \mathcal{T}(E_{ij}) \tag{2}$$

which gives reasonably accurate results when compared to QM calculations [5], [6]

Although the definition of the tunneling probability of a quasibound state faces some conceptual difficulties [4], [5] and we used a plane wave approximation for a particle decaying out of the confining potential, the results are not significantly affected by this assumption, as it will be proven by comparison with experimental results. In our approach, a transfer matrix formalism [5] based on Airy functions is used for calculating the tunneling probability, which is readily applicable to multilayer gate stacks. A single pair of Airy functions is associated to the wavefunction corresponding to each dielectric layer and the usual matching conditions are applied for each physical material interfaces. This yields a compact quasi-analytical expression [7], which captures the essential features of tunneling through a thin barrier with potential

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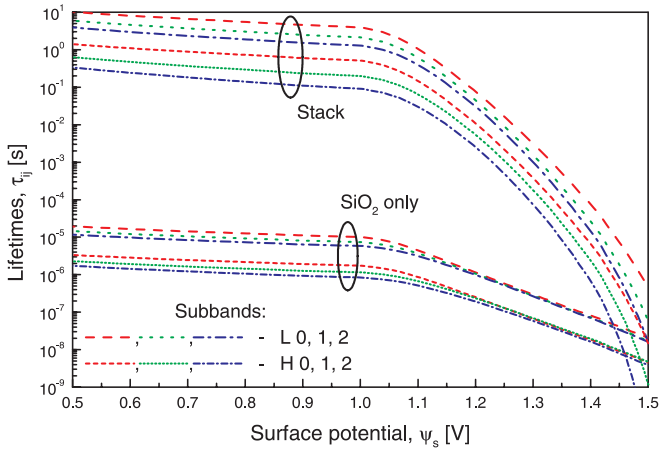

Fig. 1. Lifetimes of the quasibound states corresponding to the first three subband energy levels of the lower (L) and higher (H) valleys for a 1.5 nm SiO_2 layer and a two layer gate stack of identical EOT versus surface potential.

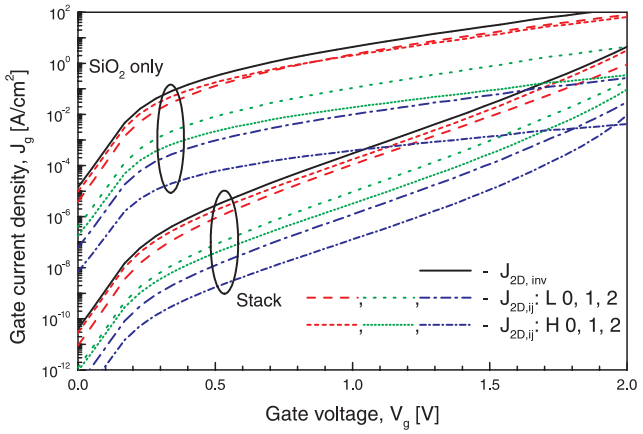

Fig. 2. Current density for a 1.5 nm SiO_2 layer and for a stack of 1.5 nm EOT with 1 nm interfacial oxide layer and contributions from different lower (L) and higher (H) energy subbands. The dominant component in the case of the gate stack comes from a subband of higher energy (H0).

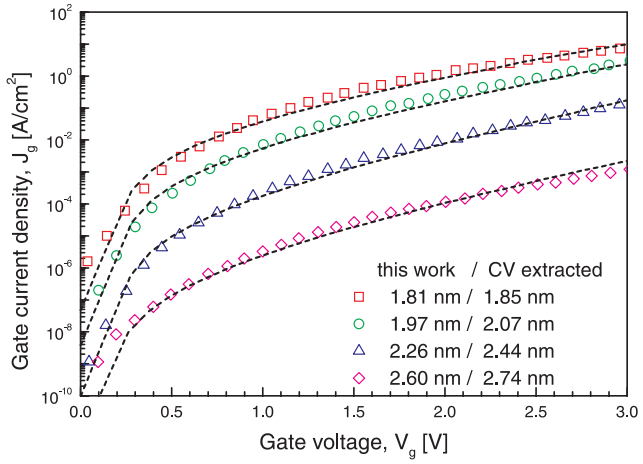

Fig. 3. Experimental gate leakage currents (symbols) and calculated curves (dashed lines). The CV extracted thicknesses are shown for comparison. The oxide effective mass was $0.5m_0$, and the barrier height 3.15 eV.

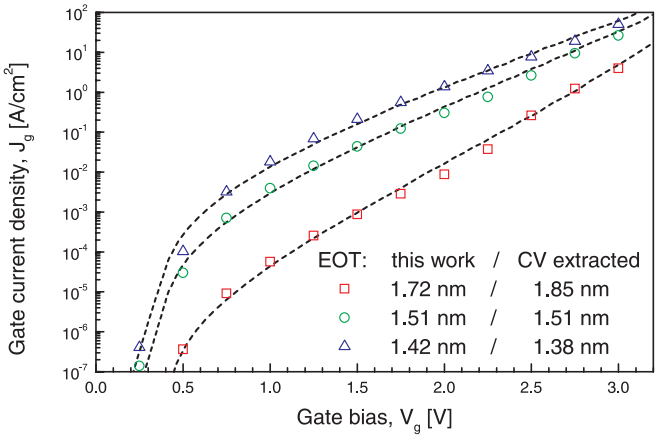

Fig. 4. Experimental gate leakage currents (symbols) and calculated curves (dashed lines) for high-k stack with Al_2O_3 [12]. The CV extracted thicknesses are shown for comparison. The oxide effective mass was $0.5m_0$, and the barrier height 3.15 eV. Material parameters for Al_2O_3 are: $k = 11$, $\Phi_B = 2.3$ eV, $m^* = 0.3m_0$.

discontinuities and does not suffer from the limitations of the more commonly used WKB based approaches [8].

The ability of the present model to describe the inverted MOS structure has been checked [9] by comparing the results obtained with solution of a self-consistent Schrödinger-Poisson solver [10].

The lifetimes of the QB states of a SiO_2 layer (Fig. 1) shows quite flat values in a range of 1 to 10 μs (for a SiO_2 thickness of 1.5 nm) before the onset of strong inversion. This is due to (i) relatively weak dependence of the energy levels on the inversion charge before the onset of strong inversion and (ii) the smaller sensitivity of the oxide voltage drop with applied bias. In strong inversion, a more pronounced decrease is observed, associated to the raising of the subband energy levels. By contrast, QB states lifetimes of a stack of identical EOT have a wider spread across the whole surface potential range and rapidly fall down in strong inversion, due to the larger differences in the effective tunneling barrier. Consequently, the dominant component of the tunneling current does not originate from the lowest energy level (Fig. 2) and subbands of higher energy levels must be accounted for when modeling the tunneling currents. The higher values of the lifetimes corresponding to the stack suggest lower tunneling currents as compared to the SiO_2

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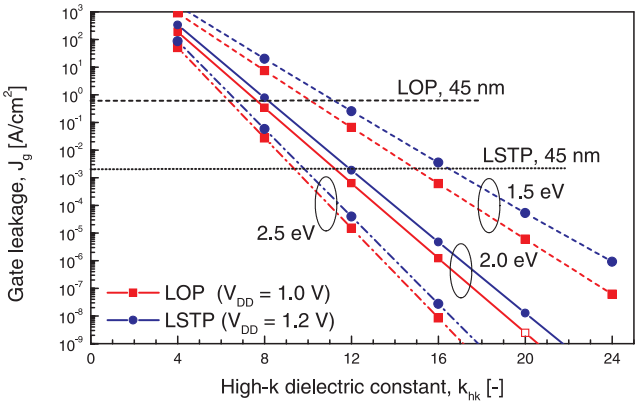

Fig. 5. Gate leakage current versus high-k dielectric constant, for different high-k barrier heights. The interfacial oxide layer thickness was fixed to 0.5 nm and the EOT of the stack is fixed at 1.5 nm. The effective masses were $0.5m_0$ (interfacial layer) and $0.3m_0$ (high-k layer).

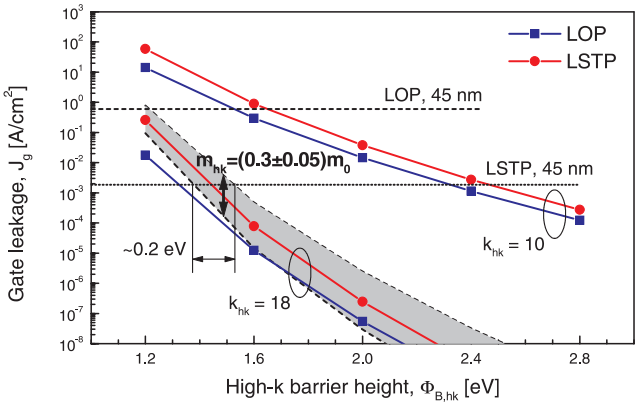

Fig. 6. Gate leakage currents versus barrier height of the high-k material. The gray strip is delimited by a high-k effective mass of $0.25m_0$ (upper limit) and $0.35m_0$ (lower limit).

TABLE I

HIGH-k MATERIAL PARAMETERS USED IN THIS WORK

Material	Al_2O_3	ZrO_2	HfO_2
Diel. const. (k [-])	10	24	22
Barrier height ($\Phi_{B,hk}$ [eV])	2.3	1.5	1.8
Eff. mass (m^*/m_0 [-])	0.3	0.2	0.2

case.

Comparison of the calculated leakage curves with experimental results [11] shows very good agreement for different oxide thicknesses (Fig. 3). The SiO_2 thickness fitting the experimental data coincided within around 1 Å precision with the values extracted from CV measurements.

Gate leakage through high-k dielectric stacks with Al_2O_3 [12] can also be fitted consistently, as shown in Fig. 4. The interfacial oxide thickness has been fixed at 0.75 nm and the high-k dielectric constant at 11, so as to agree with the CV extraction results. The remaining relevant high-k parameters were then extracted from matching calculated curves to experimental data.

III. DISCUSSION

In the following section, the impact of the high-k material parameters on the gate leakage originating from the inversion layer is discussed.

Increasing the dielectric constant (k_{hk}) of the high-k material exponentially reduces the leakage (Fig. 5) as expected. However, depending on both high-k dielectric constant and barrier height ($\Phi_{B,hk}$) several materials can be ruled out, e.g. a 2 eV high-k material will fail to meet the ITRS specifications [1] if it does not have a dielectric constant higher than about 12.

Although gate leakage dependence on the $\Phi_{B,hk}$ is less sensitive (Fig. 6), gate current variations of over 6 orders of magnitude are still possible in a barrier height range of less than 2 eV. A good high-k material should have parameters below the dashed lines in Figs. 5,6. Projections of the scalability of the high-k materials is affected by the uncertainty in the effective mass (Fig. 6) of the high-k material: nearly 15 % effective mass variation may change the currents over one order of magnitude. Reversely, the allowed gate leakage from the 45 nm LSTP node shifts the limit of the required barrier height with around 0.2 eV. The influence of the

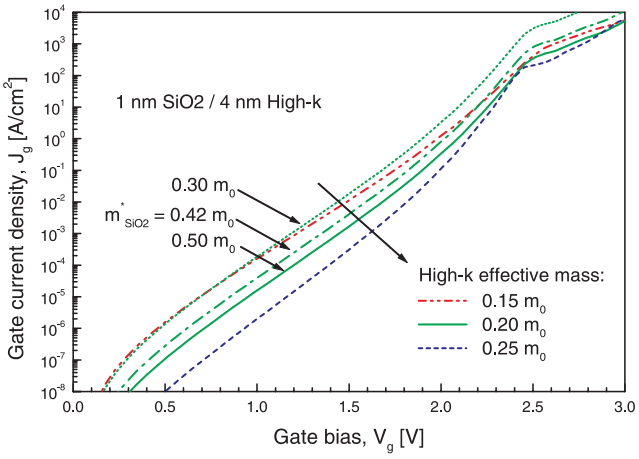

Fig. 7. Influence of the effective masses of the SiO_2 and the high-k dielectrics on the tunneling current. The high-k barrier height and dielectric constant correspond to HfO_2, as given by Table I.

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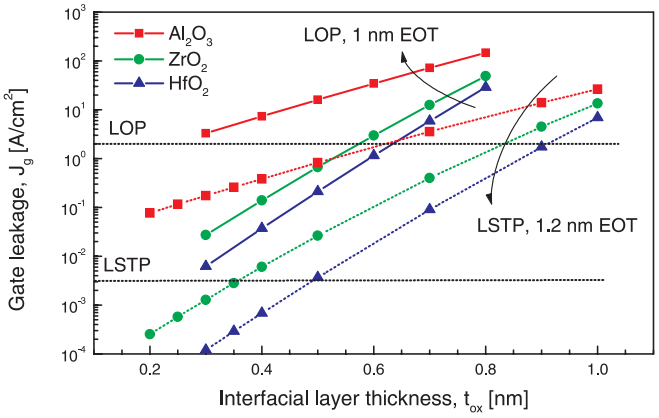

Fig. 8. Influence of the interfacial oxide layer thickness on the gate leakage, 35 nm node. The current is extracted at 0.9V (LOP) and 1.1V (LSTP). Material parameters are taken as shown in Table I.

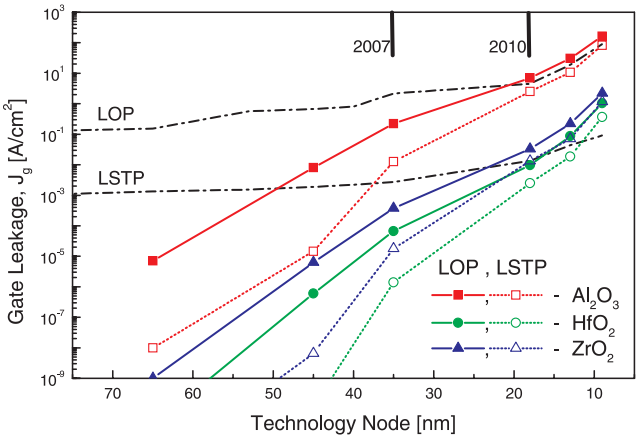

Fig. 9. Scalability of different high-k dielectrics assuming a 0.3 nm interfacial layer for LSTP (triangles) and LOP (squares) nodes. HfO_2 and ZrO_2 may fulfill the ITRS specs till the end of the roadmap.

effective mass on the tunneling current is also illustrated in Fig. 7. Decreasing the effective mass of the high-k material determines an increase of the tunneling current. This increase tends to attenuate with higher gate biases, becoming less important for very high biases, when tunneling electrons enter the conduction band of the high-k material. However, in ultrathin high-k gate stacks, this condition is usually not reached. The effective mass of the interfacial layer gives a similar dependence, but uniformly extended along the whole gate bias range.

The interfacial oxide layer is a key factor: every 1 Å of SiO_2 increase may cause up to 1 order of magnitude increase in the tunneling current corresponding to the supply voltage bias (Fig. 8). High-k stacks with Al_2O_3 do not fulfill the specifications of the 35 nm LSTP node and beyond, even if the interfacial oxide layer is completely eliminated. However, elimination of the interfacial layer might only be necessary for end of the roadmap nodes if ZrO_2 and HfO_2 are used as high-k dielectrics (Fig. 9).

IV. Conclusion

We investigated the gate leakage due to electrons tunneling from the inversion layer of a MOS structure with high-k gate dielectrics using a simple and reliable tunneling current model. Lifetimes of the QBS states are calculated within a semiclassical framework. Necessity of including tunneling from higher energy subbands has been demonstrated. All the high-k material parameters are critical in achieving the ITRS requirements. The barrier height of the high-k material may cause orders of magnitude of current variation and consequently restrict the use of several high-k materials in spite of their high value of the dielectric constant. Furthermore, projections of the high-k scalability are affected by the high-k effective mass and the interfacial oxide layer must be maintained at a very low value to meet the ITRS specifications.

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