Physical Compact Model for Threshold Voltage in Short-Channel Double-Gate Devices

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Abstract- **Compact physics/process-based model for threshold voltage in double-gate devices is presented. Drain-induced barrier lowering and short-channel-induced barrier lowering models for double-gate and bulk-Si devices are derived. The validity and predictability of the models are demonstrated and confirmed by numerical device simulation results for extremely scaled (L_{eff} = 25 nm) double-gate and bulk-Si devices.**

I. INTRODUCTION

Due to the excellent control of short-channel effects (SCEs), double-gate (DG) MOSFETs [1] can be scaled beyond bulk-Si (or PD/SOI) CMOS with improved device/circuit performance as the end of ITRS roadmap [2] is approached. However, SCEs in DG MOSFETs could arise by the perturbation of the lateral potential profile, which would yield drain-induced barrier lowering (DIBL) and short-channel-induced barrier lowering (SCIBL). Therefore, it is important to understand these effects in developing a short-channel threshold voltage (V_t) model for DG devices. In this paper, the long-channel V_t for DG devices, including channel-doping dependency of V_t, is analyzed, and then DG DIBL and SCIBL effects are modeled. A compact physical V_t model is introduced for short-channel double-gate (DG) devices. The V_t model is presented with only process-based parameters. This insightful work would be useful for developing SPICE-compatible DG device model [3] and optimizing DG device/circuit.

II. LONG-CHANNEL THRESHOLD VOLTAGE

The DG device structure is illustrated in Fig. 1. The long-channel V_t for asymmetrical (n^+/p^+ polysilicon gate) DG nMOSFET is physically derived with only four key process-based device parameters, namely front-gate oxide thickness (t_{oxf}) and back-gate oxide thickness (t_{oxb}), Si-film thickness (t_{Si}), and channel-doping density (N_A):

$$V_{t(asym)} = \frac{E_g}{2q} + \phi_B + \frac{(\Phi_{GfS} + r\Phi_{GbS}) - \left(\frac{Q_b}{C_{oxf}} - r\frac{Q_b}{2C_{Si}}\right)}{1 + r} \qquad (1)$$

where E_g is the band gap, $\phi_B = (k_BT/q)\ln(N_A/n_i)$ is the film-body Fermi potential in p-type Si, $r = 3t_{oxf}/(3t_{oxb} + t_{Si})$ is the gate-gate coupling factor [4], $\Phi_{GfS} = -E_g/2q - \phi_B$ and $\Phi_{GbS} = E_g/2q - \phi_B$ are the front and back gate-body work-function differences [5], $Q_b = -qN_At_{Si}$ is the depletion charge density, $C_{oxf} = \varepsilon_{oxf}/t_{oxf}$ is the front-gate oxide capacitance, and $C_{Si} = \varepsilon_{Si}/t_{Si}$ is the Si-film capacitance. For symmetrical DG device, the device parameters are identical for the front and back channels and gates, hence setting $\Phi_{GfS} = \Phi_{GbS}$ and $t_{oxf} = t_{oxb}$ for r in (1) yields the analytical $V_{t(sym)}$.

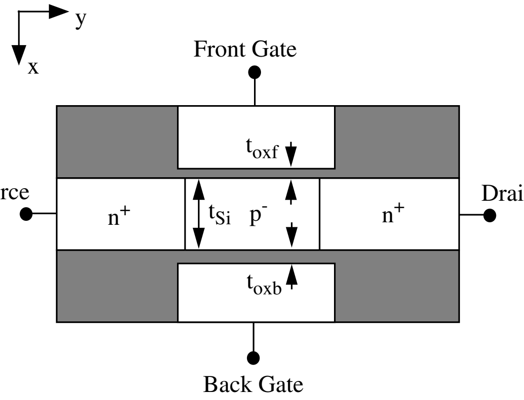

Fig. 1. The double-gate (DG) nMOSFET structure. For the asymmetrical device, the front and back gates are n^+ and p^+ polysilicon, respectively. For the symmetrical device with intrinsic-Si or lightly-doped film body, the gates should have near-mid-gap work functions for V_t control.

Fig. 2 shows MEDICI [6]-predicted current-voltage characteristics for the asymmetrical nMOSFET at low V_{DS} (= 0.05 V); V_t can be estimated by linear extrapolation at the maximum value of transconductance, $g_m = dI_{DS}/dV_{GS}$. The model prediction is confirmed by MEDICI-simulated results in Fig. 3. Fig. 4 shows model-predicted V_t vs. channel-doping density (N_A) for asymmetrical nMOSFETs. As N_A is increased, ϕ_B in (1) is increased, but it does not effect V_t unless Q_b terms are significant because the value of $(\Phi_{GfS} + r\Phi_{GbS})/(1 + r)$ is decreased by the same amount as the increase of ϕ_B. Note that changing channel-doping type from N_A to N_D in the Si film of

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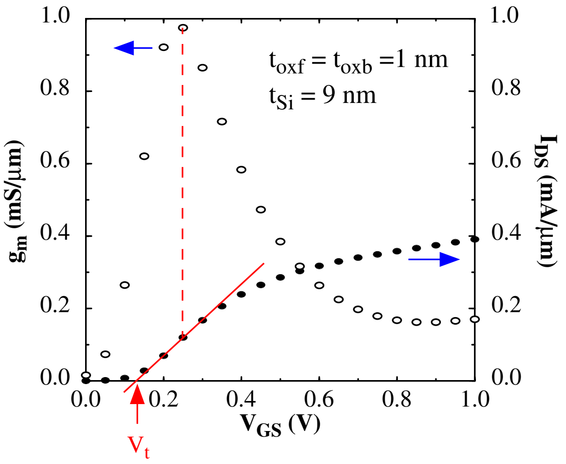

Fig. 2. MEDICI-predicted I_{DS} and transconductance (g_m) vs. V_{GS} characteristics of the asymmetrical DG nMOSFET at V_{DS} = 0.05 V; V_t is estimated by linear extrapolation at the maximum value of g_m.

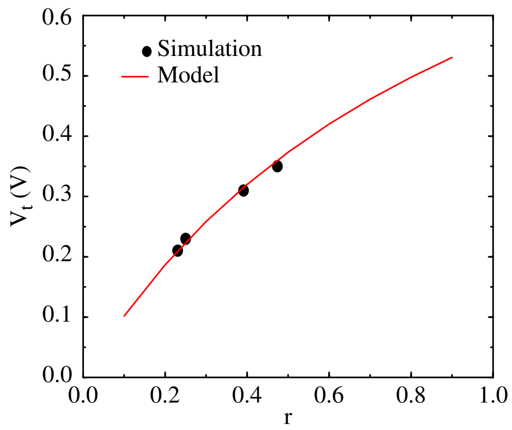

Fig. 3. V_t model (based on (1)) and MEDICI-simulated results for long-channel asymmetrical nMOSFETs with varying r = $3t_{oxf}/(3t_{oxb} + t_{Si})$.

DG nMOSFETs does not effect on DG device characteristics based on (1).

III. DIBL

In several respects, DG MOSFETs have much less severe SCEs than conventional bulk-Si MOSFETs. In DG devices, the electric field generated by the drain is better screened from the source end of the channel, due to the two-gate control. The lightly-doped and/or thin body in DG devices yields negligible depletion charge shared by the gates. However, SCEs in DG MOSFETs could arise by perturbation of lateral potential profile, which yields DIBL.

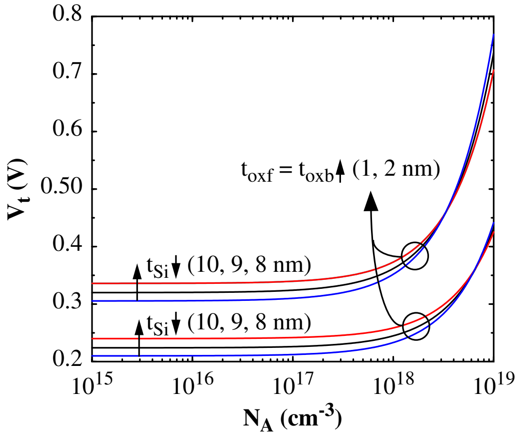

Fig. 4. Model-predicted V_t vs. channel-doping density (N_A) for asymmetrical nMOSFETs. V_t is increased as t_{Si} is decreased and $t_{oxf} = t_{oxb}$ is increased.

The DIBL model is derived as with only process-based parameters based on two-dimensional (2-D) Laplace's equation, Gauss's law, and physical approximations

$$\Delta\psi_{sf(DIBL)}^{bulk} \cong \frac{3t_d t_{ox} V_{DS}}{L_{eff}^2(1+\alpha)} \qquad (2)$$

and

$$\Delta\psi_{sf(DIBL)}^{DG} \cong \frac{3t_{Si} t_{oxf} V_{DS}}{L_{eff}^2} \qquad (3)$$

where t_d is the depletion width and $\alpha = 3t_{ox}/t_d$ [7]. The assumed source-to-drain profile (in y) is shown in Fig. 5, which defines that the metallurgical channel length (L_{met}) is 18 nm, but the effective channel length (L_{eff}) is 25 nm [5]. Fig. 6 shows MEDICI-predicted ΔV_t between V_{DS} = 0.05 V and 1 V versus L_{eff}, compared with the model predictions based on (2) and (3). From the relation between $\Delta\psi_{sf}$ and $\Delta V_{t(DIBL)}$, the DIBL-induced threshold shift can be analyzed as $\Delta V_{t(DIBL)} \cong (dV_{GS}/d\psi_{sf})\Delta\psi_{sf(DIBL)}$. The models are quite consistent with MEDICI-simulated results for bulk-Si and DG devices. Note that DIBL is comparable in asymmetrical and symmetrical DG devices, but is dramatically reduced compared with that in the bulk-Si device.

IV. SCIBL

Due to the much reduced depletion charge for the lightly-doped and/or ultra thin Si-film body, DG device is immune of charge-sharing effect, a significant factor of V_t roll-off for bulk-Si or PD/SOI devices. However, it has been shown by a device simulation that V_t of DG device is a function of L_{eff} [8]. This is

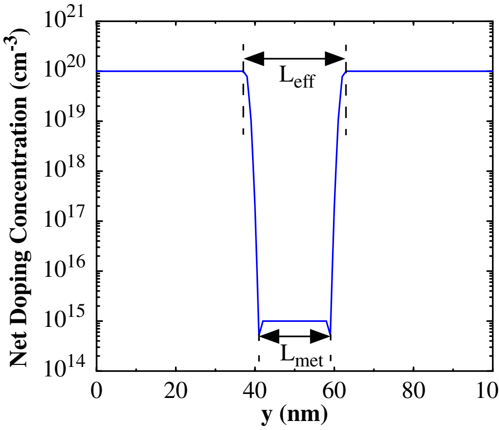

Fig. 5. MEDICI-predicted source-to-drain doping profile for the asymmetrical and symmetrical DG nMOSFETs: L_{eff} = 25 nm and L_{met} = 18 nm.

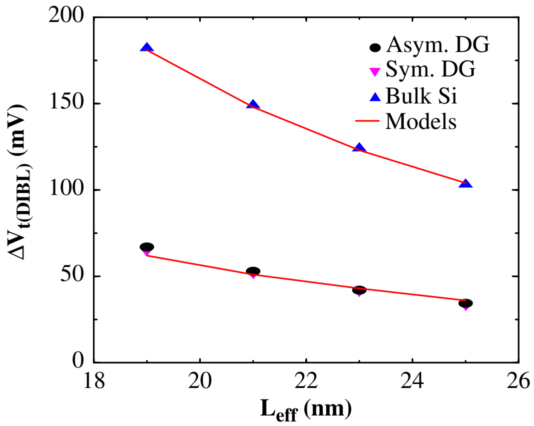

Fig. 6. MEDICI-predicted $\Delta V_{t(DIBL)}$ (defined as parallel shift in I_{DS}-V_{GS} curve between V_{DS} = 0.05 V and 1.0 V) vs. L_{eff} characteristics for the bulk-Si, asymmetrical DG, and symmetrical DG nMOSFETs, which have equal I_{off} for L_{eff} = 25 nm. DG devices have equal $t_{oxf} = t_{oxb}$ = 1.5 nm and t_{Si} = 5 nm. Models are based on (2) and (3).

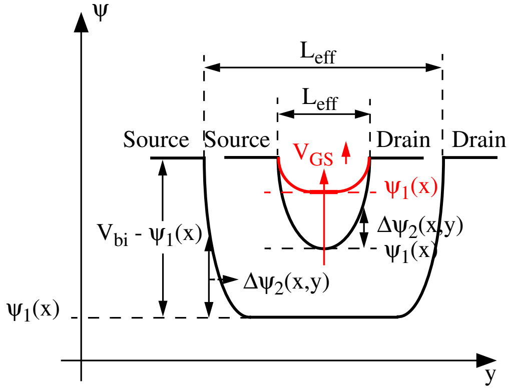

Fig. 7. Analysis for longitudinal electric potential variations of a long- and an extremely short-channel nMOSFETs for V_{DS} = 0; $\psi(x,y) = \psi_1(x) + \Delta\psi_2(x,y)$ where $\psi_1(x)$ is a 1-D potential and $\Delta\psi_2(x,y)$ is an 2-D incremental potential, and V_{bi} is a built-in potential of source-body junction. As L_{eff} increases, $\Delta\psi_2(x,y) = 0$ occurs for more y values. As V_{GS} increases, $\Delta\psi_2(x,y)$ decreases.

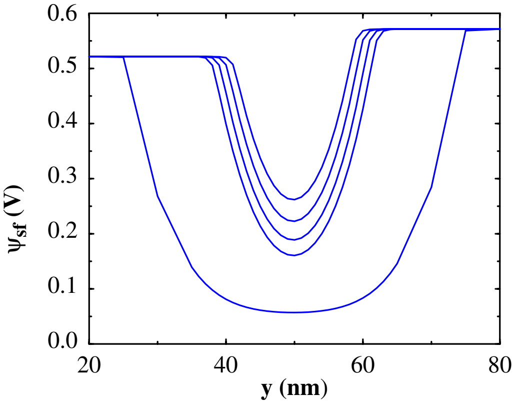

Fig. 8. MEDICI-predicted longitudinal electric potential profile of a long- and an extremely short-channel nMOSFETs for V_{DS} = 0.05 V. Note that E_y at the source is not significantly changed as L_{eff} decreases.

due to a significant phenomenon for extremely scaled device (L_{eff} < 50 nm) called short-channel-induced barrier lowering (SCIBL).

Fig. 7 depicts longitudinal electric potential variations for a long- and an extremely short-channel nMOSFET. The potential for V_{DS} = 0 is written as $\psi(x,y) = \psi_1(x) + \Delta\psi_2(x,y)$ where $\psi_1(x)$ is a one-dimensional (1-D) potential and $\Delta\psi_2(x,y)$ is an incremental potential induced by 2-D SCEs. For extremely scaled L_{eff}, $\Delta\psi_2(x,y)$ is zero only near $y = L_{eff}/2$ as shown in Fig. 7. Note that this situation occurs even for well-designed devices with L_{eff} < 25 nm, based on MEDICI-simulated results as shown in Fig. 8, and it can be called short-channel-induced barrier lowering (SCIBL). The region where $\Delta\psi_2(x,y)$ is not zero, induces less vertical controllability or more 2-D SCEs. As V_{GS} is increased, $\Delta\psi_2(x,y)$ is reduced as indicated in Fig. 8; hence two gates in DG devices enable better control of SCEs. 2-D Laplace's equation, Gauss's law, and physical approximations yield compact SCIBL model as

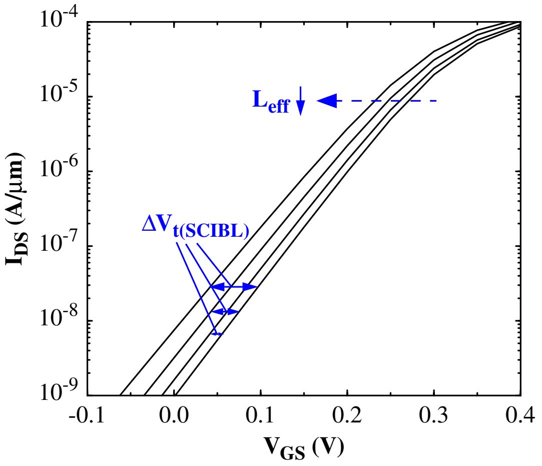

Fig. 9. MEDICI-predicted subthreshold current-voltage characteristics of (L_{eff} = 25, 23, 21, 19 nm) asymmetrical DG nMOSFET at V_{DS} = 0.05 V.

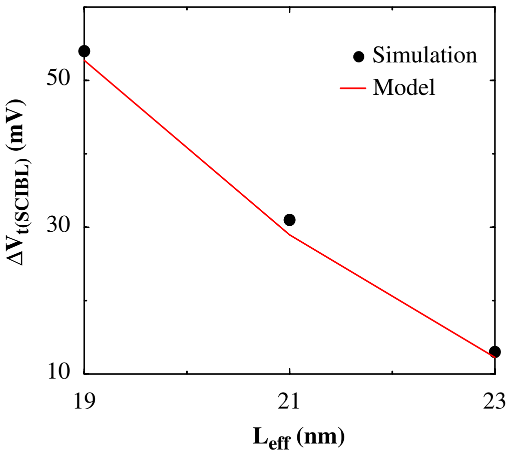

Fig. 10. MEDICI-predicted $\Delta V_{t(SCIBL)}$ vs. L_{eff} characteristics. Note that $\Delta V_{t(SCIBL)}$ is defined as a parallel shift of the I_{DS}-V_{GS} curve between L_{eff} = 25 nm and the shorter L_{eff} in Fig. 9.

$$\Delta\psi_{sf(SCIBL)}^{bulk} \cong \frac{9t_d t_{ox}(E_g/2q)}{L_{eff}^2(1+\alpha)} \qquad (4)$$

and

$$\Delta\psi_{sf(SCIBL)}^{DG} \cong \frac{9t_{Si} t_{oxf}(E_g/2q)}{L_{eff}^2} \ . \qquad (5)$$

Fig. 9 depicts MEDICI-predicted subthreshold current-voltage characteristics of asymmetrical DG nMOSFET for low V_{DS}. Fig. 10 shows the models are quite consistent with MEDICI-simulated results for bulk-Si and DG devices. Note that SCIBL is comparable in asymmetrical and symmetrical DG devices, but is dramatically reduced compared with that in the bulk-Si device. Now, from (1), (3), and (5), V_t for short-channel asymmetrical DG nMOSFET would be analytically expressed as

$$V_{t(asym)} = \frac{E_g}{2q} + \phi_B + \frac{(\Phi_{GfS} + r\Phi_{GbS}) - \left(\frac{Q_b}{C_{oxf}} - r\frac{Q_b}{2C_{Si}}\right)}{1+r} - \frac{3t_{Si}t_{oxf}V_{DS}}{L_{eff}^2} - \frac{9t_{Si}t_{oxf}(E_g/2q)}{L_{eff}^2} \ . \qquad (6)$$

By setting $\Phi_{GfS} = \Phi_{GbS}$ and $t_{oxf} = t_{oxb}$ in r, (6) could yield V_t for short-channel symmetrical DG device.

V. CONCLUSIONS

Reliable compact physical V_t models are presented for extremely scaled DG devices and bulk-Si devices with process-based parameters. This work also identifies SCEs for future scaled devices and provides the methodology for physical DG device modeling and the insight for DG device/circuit design optimization.

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