Grain Boundary Effects on Subthreshold Behaviour in Single Grain Boundary Nano-TFTs

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***Abstract*— A simulation model for deep trap states at grain boundaries in Poly-Si TFTs is developed. The model is used for simulation of single GB TFT devices with sub micron channel lengths. The transport physics is clarified and it is found that in short channel devices ($L_{eff} < 100$nm) the single GB TFT shows improved subthreshold behaviour compared to its SOI equivalent.**

I. Introduction

Poly-Silicon thin-film transistors (TFTs) have been studied extensively in recent years for their application in flat panel active matrix liquid crystal displays(AMLCD). In AMLCD applications the gate length of the TFT is typically greater than one micron and therefore a large number of grain boundaries (GBs) are present in the TFT channel. Conventionally, the effect of the GBs is considered to reduce the electron mobility below the bulk-single crystal value. In such an analysis the discrete properties of individual GBs are not considered. Much effort has been made to increase both the grain size and therefore the mobility in poly-Si films. Some success has been found using modern Metal-Induced Lateral Crystallization (MILC) [1] and excimer laser annealling techniques [2].

For applications in 3D VLSI the device must be scaled to much smaller dimensions. In scaling the channel of the device down to the nanometre regime - a length and width comparable to the poly-Si grain size - it is important to understand the effects of discrete GBs on conduction [3].

According to the theory by Seto [4], electrons are trapped at the grain boundaries depleting the surrounding regions making them positively charged and making the boundary itself negatively charged. This causes band bending resulting in a potential barrier forming at the GB which impedes electron transport. Increasing the number of carriers in the film acts to reduce the depletion region surrounding the GB and therefore reducing the barrier height.

We aimed to investigate using 2D device simulation whether the GBs could have a positive as well as negative effect on the electrical characteristics of aggressively scaled poly-Si TFTs.

II. Device Modeling

The basic drift-diffusion transport equations used are the same as those of a single crystal device except that the trapped charges within the grain boundary region are included in Poisson's equation. The model for carrier emission and absorption processes proposed by Shockley-Read-Hall is used as the trap model at the GBs. The negative charge at the grain boundary can be calculated as

$$N^- = \frac{n/C_p + p_1/C_n}{(n+n_1)/C_p + (p+p_1)/C_n} N_T \tag{1}$$

Where n and p are the electron and hole densities, N_T the trap density, C_n and C_p are the electron and hole capture rates. Parameters n_1 and p_1 are defined by

$$n_1 = n_i exp[(E_t - E_i)/kT] \tag{2}$$

$$p_1 = n_i exp[(E_i - E_t)/kT] \tag{3}$$

where n_i is the intrinsic carrier density and E_i is the intrinsic Fermi level.

Adding the negative charge given in Eq. (1) to the space charge originating from donors(N_D) and acceptors(N_A) we get the total charge Q.

$$Q = q(N_D - N_A - N^- - n + p) \tag{4}$$

and therefore Poisson's Equation can be written as

$$\nabla(\epsilon \nabla \Psi) = q(N_D - N_A - N^- - n + p) \tag{5}$$

The current continuity equations are given by

$$\nabla J_n = q.R \tag{6}$$

$$\nabla J_p = -q.R \tag{7}$$

where J_n and J_p are the electron current density vector and the hole current density vector, and R is the Shockley-Read-Hall recombination rate.

TABLE I

TABLE OF PARAMETERS FOR THE SIMULATED DEVICE

Parameter	Range of Values
Channel Length L_{eff}	50nm-400nm
Gate Oxide Thickness t_{ox}	10nm
Channel Doping Concentration N_{D}	$1\text{x}10^{17}cm^{-3}$
Source,Drain and Gate Doping Concentration	$1\text{x}10^{21}cm^{-3}$
Density of Deep Acceptor like Traps N_{T}	$1\text{x}10^{13}cm^{-2}$
Trap Energy Level Relative to Conduction Band E_{T}	0.51eV
Capture Rate for Holes C_{p}	$1\text{x}10^{-8}cm^{3}/sec$
Capture Rate for Electrons C_{n}	$1\text{x}10^{-8}cm^{3}/sec$

The current density equations are given by

$$J_n = -q\mu_n n \nabla \phi_n \tag{8}$$

$$J_p = -q\mu_p p \nabla \phi_p \tag{9}$$

where μ_n and μ_p are the electron and hole mobilities and ϕ_n and ϕ_p are the electron and hole quasi-Fermi potentials, respectively. These equations are discretised using the finite difference method and then solved iteratively. In our modelling we only have trap states present in the GB region and not in the bulk which is treated as single crystal silicon. A model of trap-to-band tunneling, for gate induced drain leakage(GIDL), is not included in the present simulation. This enables the effect of the presence of the GB, on the subthreshold characteristics, to be observed without being obscured by high leakage currents.

The device structure used in our simulations is shown in Fig. 1. and the device parameters in Table I. When modelling TFTs with a large number of GBs, trap states are considered to be distributed evenly over the whole channel. In our modelling we only have trap states present in the GB region and not in the bulk which is treated as single crystal silicon.

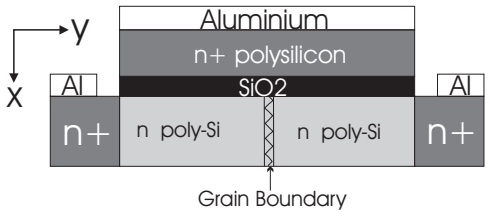

Fig. 1. Structure used for the TFT simulation

III. SIMULATION RESULTS

A. Dynamic Threshold Behaviour in TFT subthreshold characteristics

As a result of the n-type doping of the channel region devices operate in accumulation mode. Thermionic emission over the GB barrier is the limiting transport process when the barrier height V_{B} is larger than the thermal voltage. When V_{B} is reduced by gate induced barrier lowering (GIGBL) to below the thermal voltage, the characteristics will become similar to those predicted by a conventional SOI MOSFET model. When the barrier height becomes greater than the thermal voltage the current flow will be reduced. Two devices were simulated, both with a channel doping density of 1 x $10^{17}cm^{-3}$, channel thickness (t_{si}) 0.05μm , channel length (L_{eff}) 0.4μm and oxide thickness (t_{ox}) 10nm. The first device has a grain boundary present in the centre of the channel and the other device uses a single crystal silicon channel.

The resulting subthreshold characteristics can be seen in Fig. 2. For a device with a grain boundary in the channel and an equivalent SOI device, the drain current (I_{d}) against the gate voltage (V_{g}) are plotted. This result is for the linear regime of the TFT with a low drain bias voltage ($V_{\text{d}} = 0.01V$).

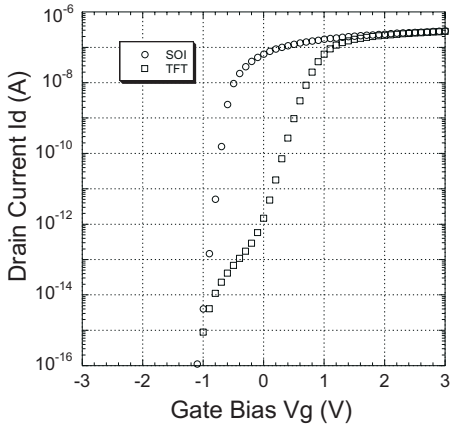

Fig. 2. A comparison of characteristics for a TFT with a single GB in the channel and single crystal SOI TFT with equal geometry.

It can be seen that the current in the TFT device appears to be suppressed around the 0V region of operation producing a dip in the subthreshold slope. When the gate voltage is highly positive ($V_{\text{g}} > 1V$) or negative ($V_{\text{g}} < -1V$) the drain current is similar to that for the SOI device. We suggest that this behaviour is made clear in our device simulations because leakage current mechanisms are not included. In a real device leakage currents of greater that $1\text{x}10^{-13}$A would hide the current suppression that results from the GB.

The results seem to show two distinct conduction effects caused by the GB. When the gate is unbiased the region in the channel surrounding the GB is close to full depletion, with all the available trapped states at the grain boundary filled. Hence the resulting potential barrier is at, or close to, its maximum height.

With increasing gate bias, the barrier is reduced close to the interface allowing more current to flow. This continues until the barrier height at the interface is smaller than the thermal voltage, at which point the barrier no longer impedes current flow and the transistor behaviour is similar to that of the SOI equivalent device.

In the subthreshold regime the presence of the barrier aids the suppression of the off current. As the bias voltage is

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made increasingly negative, the potential barrier at first acts to suppress the current flow in the channel; resulting in a lower drain current than is present in the SOI MOSFET under this gate bias. Later, the modulation of the channel potential by the gate becomes dominant and the potential barrier formed by this mechanism becomes equal to, or greater than, the GB barrier. At this point the characteristics again match those of the SOI device.

B. Comparison with Experiment

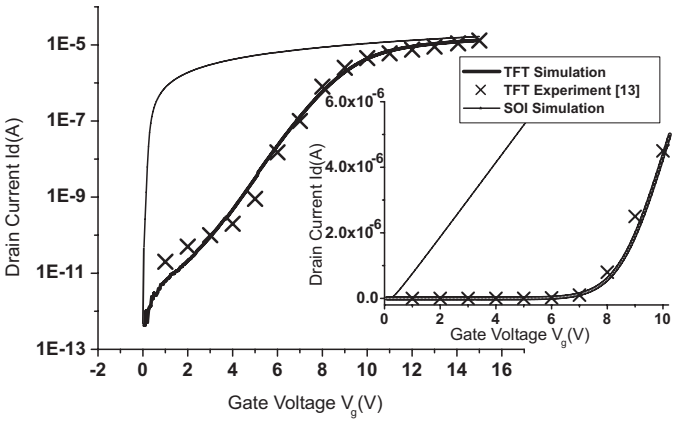

Fig. 3. Comparison between simulated and experimental [5] Id-Vg characteristics for a p-channel inversion mode TFT with two lateral GBs in the channel region on both logarithmic and (inset) linear scale.

An SOI transistor with two GBs in the channel region perpendicular to the current flow is described in [5]. The device is an inversion mode transistor with a 5x10$^{16}cm^{-3}$ p-doped channel region with channel length L_{eff}=14μm. Measurements indicate current suppression at a gate bias of 5V which the author attributed to leakage currents. We believe the cause to be GIGBL with a gate bias of greater than 5V required to lower the GB barriers in the channel.

To validate our modelling technique we simulated this device and compared the results with those measured by experiment [5]. Comparing the experimental and simulation results in Fig. 3 we can see there is good agreement on both linear and logarithmic scales. This result was found by setting $E_{\text{T}} = 0.65eV$, N_{T}=6x10$^{19}cm^{-3}$, which is in agreement with the experimentally measured values in [6] and giving the silicon regions a reduced mobility of $\mu_{\text{n}} = 600cm^2/V.s$. Capture rates and source and drain doping were as given in Table 1.

C. Scaling of the channel length into the nanometre regime

In order to investigate the usefulness of the GB effects a range of simulations were performed comparing SOI devices and single GB TFT devices with equal geometries. According to SOI scaling theory [7], reducing the channel length L_{eff}, while keeping t_{si} constant will result in degradation of the transistor performance as a result of short channel effects.

Simulation results are shown in Fig 4. It is found if we decrease L_{eff} while keeping t_{si}=50nm that the subthreshold

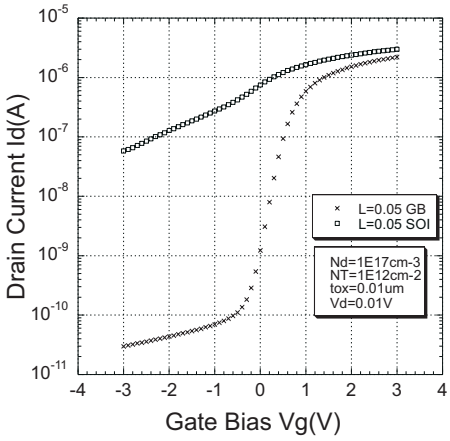

Fig. 5. Here the channel length is scaled down to 50nm. By direct comparison of the Id-Vg characteristics of a single GB TFT and a same geometry SOI device it is easy to see that the GB improves the subthreshold behaviour.

slope for the TFT with the GB varies very little above 0V for devices with channel length as small as 50nm. Fig. 5 illustrates this behaviour by comparing the SOI and TFT characteristics for a device with L_{eff}=50nm. The TFT characteristics are clearly superior to the SOI characteristics for a device with these dimensions. For short channel length L_{eff}, improved subthreshold behaviour is found by having a GB present at the cost of an increased threshold voltage. The GB acts to suppress the off current, while the need to lower the potential barrier resulting formed at the GB, results in a larger threshold voltage in the TFT devices.

D. Analysis of 50nm single GB TFT

To investigate how having the GB in a short channel device results in improved device characteristics, the 2D surface potential for both SOI and TFT devices was plotted for three gate biases in the subthreshold regime (Fig 6).

It can be seen in Fig 6(b) that even at zero bias there is a large potential barrier in the TFT device which increases in size as the gate bias becomes increasingly negative. In contrast for the SOI device there is no barrier at 0V (Fig. 6(f)) and under increasingly negative bias a small barrier is formed. In the short channel device the gate is unable to modulate the barrier potential sufficiently to suppress carrier transport, in contrast to the TFT where the barrier at the GB aids in suppressing the OFF current.

IV. Conclusion

A simulation model for TFT devices with GBs of finite area has been developed. The model uses Shockely-Read-Hall recombination and emission processes from trap states present in the band gap of the device as it's basis.

SOI and single GB TFT devices of varying channel length have been simulated and compared. It has been found that for short channel devices in the linear regime the single GB device has superior subthreshold characteristics.

Looking at the 2D surface potential in the channel of a 50nm TFT and SOI device, has shown that in the TFT the

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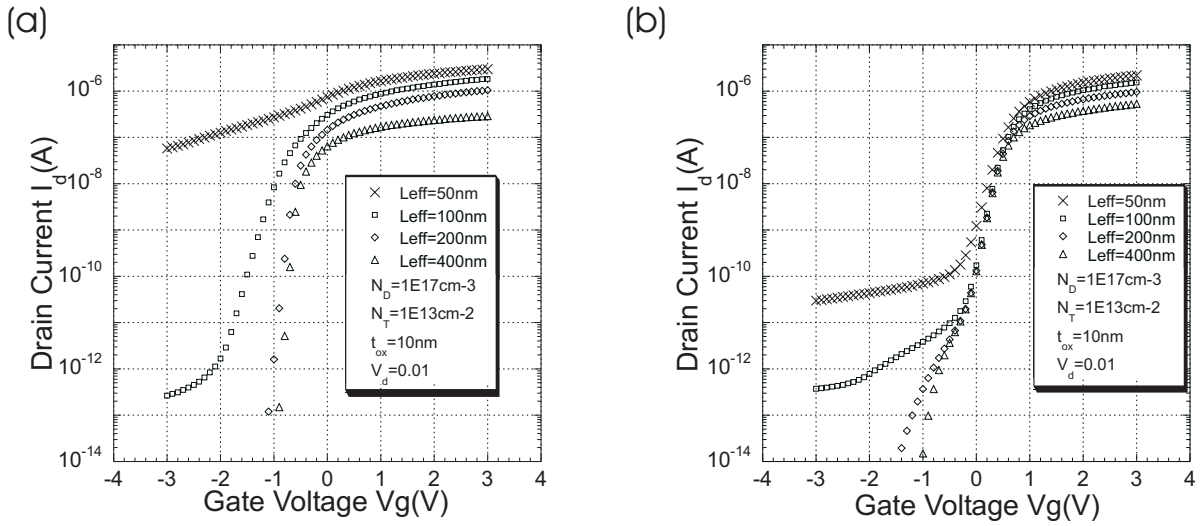

Fig. 4. (a) SOI MOSFET (b) single-GB TFT - The single GB TFT shows better subthreshold behaviour when the channel length is below 100nm

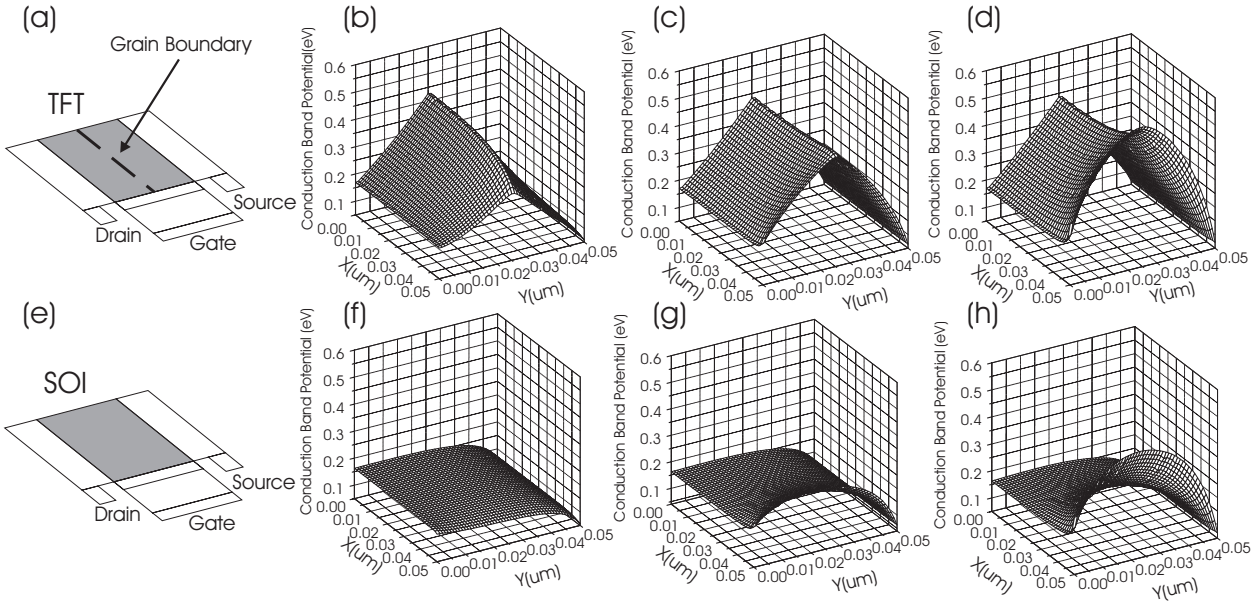

Fig. 6. Device cross-section of (a) 50nm TFT (e) and SOI equivalent with modelled region of channel shaded. Conduction band potential for (b and f) V_g=0V , (c and g) V_g=-0.5V, (d and h) V_g=-1.0V

potential barrier at the GB aids in suppressing the off current and therefore gives improved performance in the subthreshold regime compared to an SOI equivalent device.

ACKNOWLEDGMENT

The authors would like to thank Prof H. Ahmed, Dr D. Hasko, Dr K.Yamaguchi, Dr T.Teshima and Prof E.C. Kan.

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