Computer Aided Design of Sub-100nm Strained-Si/Si $_{1-x}$Ge$_x$ NMOSFET through Integrated Process and Device Simulations

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Abstract - Integrated process and device simulations were performed to design sub-100nm Strained-Si/Si$_{75}$Ge$_{25}$ devices. The process and device models were carefully calibrated according to various physical and electrical device characterizations. It is observed that the dopant behavior is highly sensitive to the presence of the SSi/SiGe heterointerface, especially when the SSi thickness is reduced below 10nm. This points to SSi thickness as a new source of process variation and careful control of the SSi layer is important to maintain consistent device performance. In addition, the Type-II energy-band alignment at the heterointerface also contributes strongly to the short-channel device behavior. This work illustrates the need for accurate heterostructure-based process and device models in order to simulate and design aggressively-scaled strained-Si devices.

I. INTRODUCTION

Interest intensifies in mobility-enhanced strained Si devices as an emerging high-performance successor to the Si Metal-Oxide-Semiconductor-Field-Effect-Transistors (MOSFETs) [1]. The technique of pseudomorphically straining epitaxial Si channels with SiGe substrates has consistently produced devices with electron mobility improvement over unstrained Si [2], [3], [4], [5]. The transition to strained-Si/SiGe (SSi/SiGe) MOSFETs from Si devices may appear to only require a substrate change in theory. In practice, due to dramatic doping differences between Si and SiGe, extensive source/drain (S/D) and channel re-engineering is necessary to achieve successful deep sub-100nm devices. Though numerous quality modeling work has been reported on dopant diffusion in SiGe [6], [7], [8] and SSi device physics [9], [10], [11], [12], [13], relatively few have discussed device design by combining the two intimately-related aspects of device design [14], [15]. In this paper, we present an integrated modeling approach, from dopant implantation and thermal processing to device simulation, that allows us to optimize short-channel control and parasitic S/D resistance in aggressively-scaled SSi devices.

II. MODELS

Dopant implantations were simulated by two-dimensional Monte-Carlo method [16] and analytic implant tables with nuclear and electronic-stopping of SiGe calibrated to Secondary Ion Mass Spectrometry (SIMS) data (Fig. 1). The coupled dopant diffusion processes during thermal steps are described by DIOS's implementation of the pair-diffusion model [17], where dopant-defect pairs and unpaired point defects are the mobile species. Transient enhanced diffusion is simulated by the addition of point defects from implant damage according to the "plus-one" model [18]. The SiGe substrate is modeled by doping Si to alloying concentrations corresponding to the Ge mole fraction, x, where the mole-fraction-dependent SSi and SiGe band gaps are according to Rieger et. al. [19]. The Ge-induced chemical and defect formation energy influences on dopant diffusivities are described by $D = D_o exp(-Q\ s/k_BT)$ [6]. Where, D_o is the dopant diffusivity in Si, s is the lattice deformation due to Ge, and Q is the change in diffusion activation energy determined from the theory of lattice expansion [20] and calibration of simulated diffusion according to SIMS characterization.

The device simulation includes a model of a Type-II heterostructure at the SSi/SiGe interface delineated by the sharp change in Ge concentration (Fig.1). The SSi/SiGe conduction and valence band offsets, ΔE_C and ΔE_V respectively, are according to Ref. [19]. Recesses into the strained-Si layer due to the gate etch, clean and spacer processing lead to non-uniformity in the strained-Si thickness along the length of the device (Fig. 1a). The recesses were replicated in the model during process simulations and the final structure was checked against Transmission Electron Microscopy (TEM) images of the devices.

A drift-diffusion approach in DESSIS [21] has been applied to model the carrier transport, where the drive current enhancement is calibrated to experiments through detailed matching of mobility and transconductance behavior. Simulations base on hydrodynamic models are also being performed as comparisons. Band-to-band tunneling according to Schenk [22] is included to account for junction leakage in addition to diode current increase arising from reduced band-gaps of SSi and SiGe.

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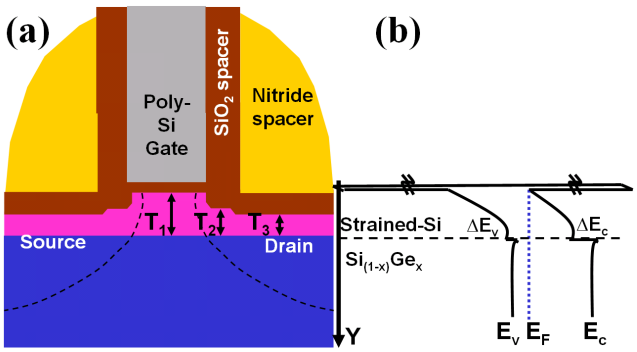

Fig. 1 (a) A schematic of gate and channel structures with exaggerated recessed features that illustrate typical differences in SSi thicknesses(T_1,T_2 and T_3) under the gate and spacer regions. (b) The energy band diagram showing the Type-II heterostructure in the vertical direction under the gate.

III. RESULTS

Figure 2 and 3 depict the SIMS and simulated As profiles after 1025°C and 900°C anneals, respectively for SiGe with 25% Ge. We see that high-temperature anneals dramatically enhances the diffusion of As in SiGe. The diffusion can be sensitive to the presence of the heterostructure and Ge distribution, leading to very different doping profiles when the diffusion occurs in the absence of the SSi layer (Fig. 2).

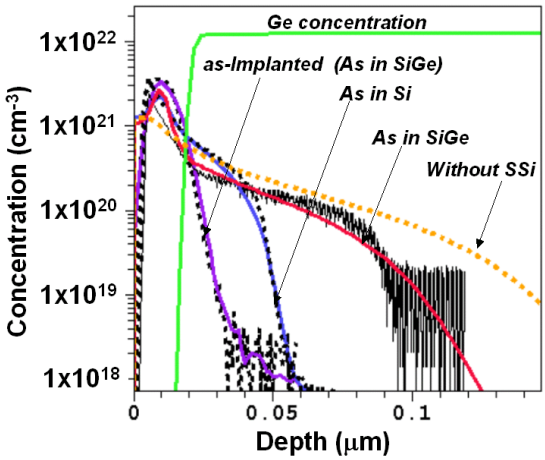

Fig. 2. Diffusion of As in Si and SSi/SiGe heterostructure after a 10-seconds 1025°C anneal (Solid:Simulated Dashed:SIMS).

When the anneal temperature is lowered to 900°C, dopant diffusion in SiGe becomes comparable to that of Si (Fig. 3). The diffusion is now relatively less sensitive to the presence of the heterostructure and more influenced by the point defect supersaturation resulting from the implants.

Figure 4 shows the B doping profiles after the same set of anneals. In this case, boron diffusion in the SiGe substrate is retarded when the anneal temperature is high and becomes comparable to the Si case when temperature is lowered.

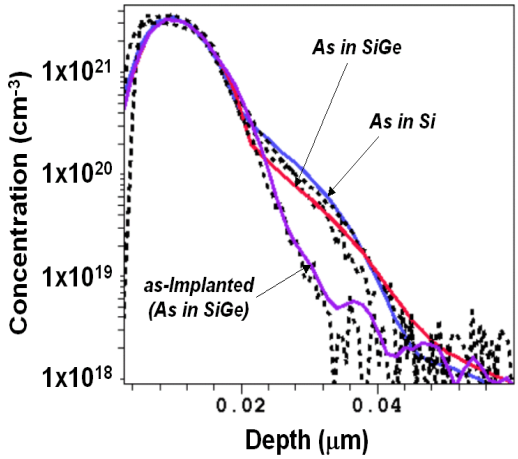

Fig. 3. Diffusion of As in Si and SSi/SiGe heterostructure after a 900°C -10sec thermal anneal (Solid:Simulated Dashed :SIMS).

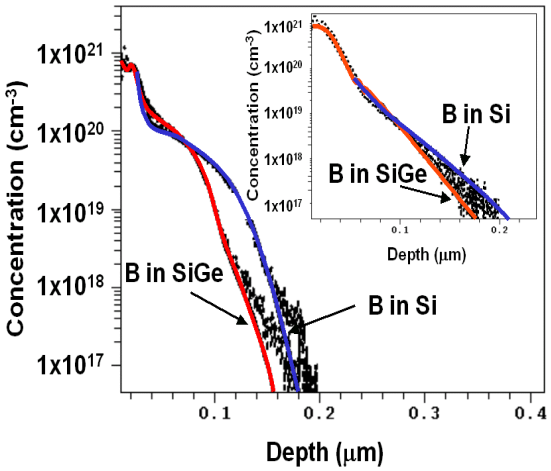

Fig. 4. Diffusion of B in Si and SSi/SiGe heterostructure after a 10-seconds high-temperature anneal (Solid:Simulated Dashed:SIMS). Inset: Dopant diffusion when anneal temperature is lowered to 900°C.

Figure 4 shows the junction profiles of a SSi device that received S/D implants meant for optimized Si devices. Due to dopant diffusivity differences across the SSi/SiGe interface, unique "bow"-shaped junctions are formed. In addition, the As S/D extensions (SDEs) are overwhelmed by the S/D doping. The physical channel defined by the S/D junctions has become narrowest away from the gate oxide-semiconductor interface, severely limiting gate length scaling by promoting the early onset of punch-through and short-channel effects. By carefully designing the implants, excessive lateral diffusion can be arrested and short-channel control can be improved in sub-100nm SSi devices, even with high-temperature anneals.

Figure 6 compares the As S/D and B halo profiles for 50nm Si and SSi devices. The SSi devices show more abrupt halo profiles due to retarded B diffusion in SiGe and deeper junctions due to enhanced As diffusion. The shallower B profile in the SSi devices requires an adjustment of the S/D extension implants to reduce excessive counterdoping of the extensions and ensure appropriate overlap with the gate.

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The differences in density of states, band-gap and band offsets contribute to a workfunction-like V_T difference between SSi and equivalent Si devices. From capacitance-voltage (C-V) measurement of long-channel devices, the V_T difference is determined to be approximately 150 mV (Fig. 7). Good agreement between measurements and simulations for the High-frequency C-V characteristic of long-channel SSi devices can be obtained when the appropriate band offsets and band-gap values are applied. The long-channel V_T of the SSi devices was found to be most sensitive to the ΔE_C and ΔE_V values. Base on simulations, a channel implant to adjust for the V_T difference has been applied.

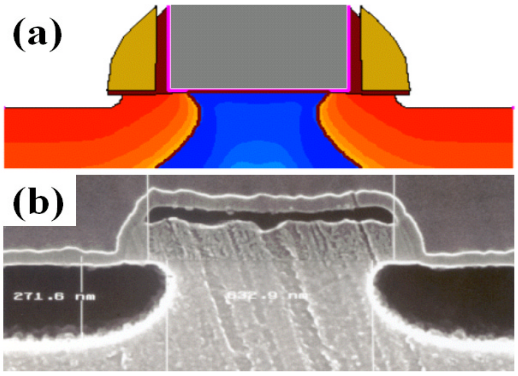

Fig. 5. (a) Simulated junction profile of a long SSi/SiGe device before S/D optimization (b) Scanning electron microscopy of a dopant-selective etched device showing the junction profile due to the SSi/SiGe heterostructure.

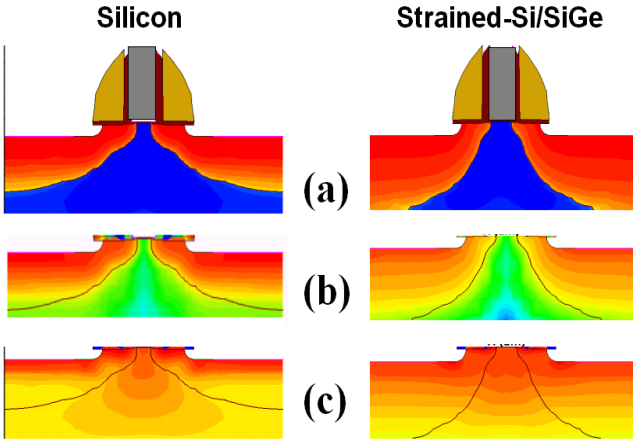

Fig. 6. (a) Net doping concentration delineating the junction profiles of small NMOS devices. (b) Contour plots of As doping. (c) Contour plots showing the B halos.

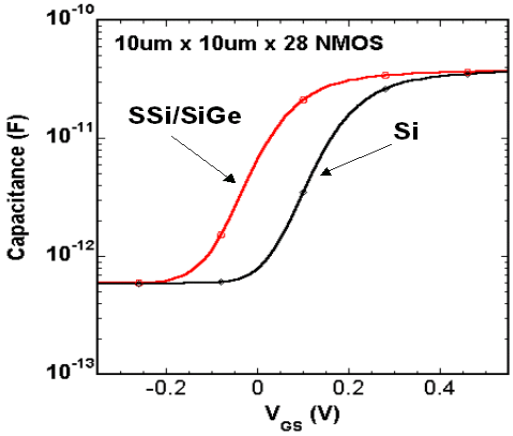

Fig. 7. (a) High-frequency C-V measurement of a 28-device array showing the V_T difference between long-channel SSi and Si devices.

Our simulations show that the thickness of the SSi layer is an important factor in determining the S/D profiles and consequently the short-channel behavior of the device. We observed that when the SSi thickness is reduced below 100 Å, the lateral diffusion of the S/D extensions increases, for a given implant and thermal anneal conditions. Figure 8 show the contour plot of the junction and halo profiles of two SSi devices with different SSi thickness, which underwent the same implant and anneal processes. The enhanced lateral diffusion leads to a reduction in physical channel length, defined by the separation between the S/D extensions (Fig. 8a). As the SSi thickness is decreased, the junctions come closer together and deepen. This is due largely to the fact that a larger portion of the S/D As dopants is located in the SiGe when the SSi is thin and more dopants undergo enhanced diffusion in the presence of Ge. In addition, the B halo distributions in the two devices are also markedly different (Fig 8 b and d) due to different amount of retardation experienced by the dopants when the SSi thickness changes. Therefore, careful design of implant depth and dose that accounts for the dopant sensitivity to the hetrojunction is needed to achieved optimum S/D junctions.

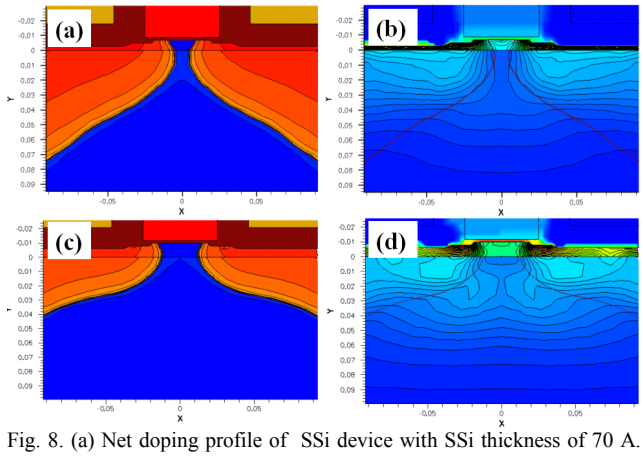

Fig. 8. (a) Net doping profile of SSi device with SSi thickness of 70 A. (b) The boron halo profile of the SSi device with 70A thick SSi . (c) Net doping profile of SSi device with SSi thickness of 100 A. (d) The boron halo profile of the SSi device with 100A thick SSi .

Figure 9 shows a plot of the drain-induced-barrier-lowering (DIBL) metric as a function of SSi thickness. DIBL which is defined by $(V_T(\text{lin}) - V_T(\text{sat}))/(1.2V\text{-}0.1V)$ where $V_T(\text{lin})$ and $V_T(\text{sat})$ are the threshold voltages when

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the device is biased at 0.1 V and 1.2 V, respectively. As the SSi thickness is thinned from 100 Å to 50 Å, DIBL increases rapidly for the 70-nm device, due to enhanced lateral diffusion of the S/D extensions. However , the changes in DIBL is negligible for the slightly longer device (L_{gate}=100nm) for the same reduction in SSi thickness. The difference in DIBL sensitivity between the shorter and longer devices can be explained by the differences in the VT-vs-L roll-off characteristic. The 70-nm and the 100-nm devices demonstrate the same DIBL when the SSi greater than 100 Å, indicating that enhanced lateral diffusion is minimized for SSi thicker than 100 Å.

We have found that the short-channel behavior of the devices is not only influenced by the location of the SSi/SiGe interface but also the band-offset at the heterojunction. When the conduction band offset ΔE_C is reduced to zero, the DIBL increases slightly, especially when the SSi is thinned which indicates that the band structure of the heterointerface helps to reduce short-channel effect. The Type-II energy band alignment at the heterointerface tends to "crowd" the current entering and leaving the channel at the source and drain regions, restricting current spreading in the S/D regions. This weak confinement due to the energy bands gives rise to effective S/D extensions that are electrostatically shallower, thereby reducing charge-sharing effects and DIBL. Consequently, the spreading resistance of the devices are also increased when they are compared to devices with ΔE_C set to zero.

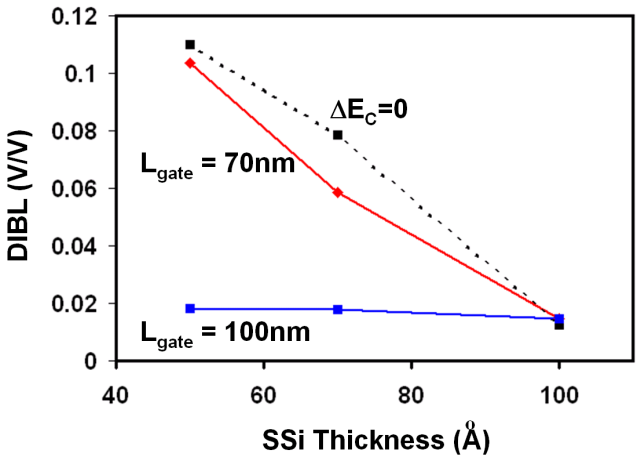

Fig. 9. DIBL metric as a function of SSi thickness. Blue curve is for a Lgate=100nm device and the red curve is for Lgate=70nm. Dashed: curve for 70nm device when ΔE_C is set to zero.

Base on learning gain from simulations on the role of strained-Si thickness with respect to dopant and device behavior, we are able to design 45-50nm devices with well-behaved short-channel characteristics. Figure 10 compares the simulated and measured characteristics of a L_{gate}=50nm SSi device with good short-channel control, exhibiting a DIBL of only 52mV/V. The SSi thickness under the gate was measured to be approximately 60 Å. The model prediction is in close agreement with the experiment except for the underestimation of junction leakage. This is due to the neglect of direct gate tunneling and dislocation defect-mediated leakage in the present model.

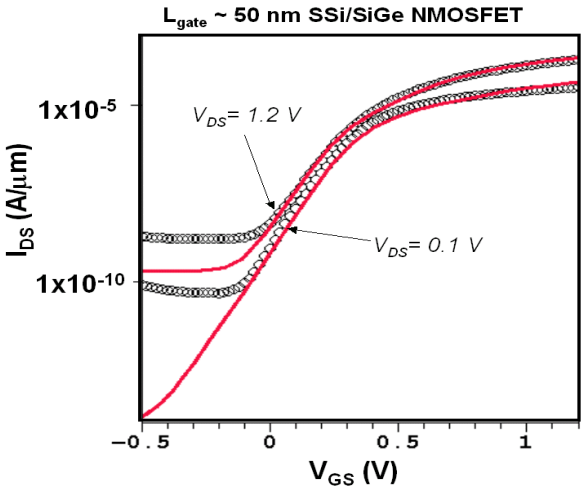

Fig. 10. Drain-current versus gate voltage characteristic of a 50nm SSi device. (Symbols: Measurement Solid: Simulation).

IV. CONCLUSION

Integrated process and device simulations were performed to design sub-100nm SSi/SiGe devices. The process and device models were carefully calibrated according to various physical and electrical characterization data of the devices. It is observed that the dopant behavior is highly sensitive to the presence of the SSi/SiGe heterointerface, especially when the SSi thickness is reduced below 10nm. This points to SSi thickness as a new source of process variation and careful control of SSi thickness is important to maintain consistent device performance. In addition, the Type-II energy-band alignment at the heterointerface also contributes strongly to the short-channel device behavior. This work illustrates the need for accurate heterostructure-based process and device models in order to simulate and design aggressively-scaled SSi/SiGe devices.

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