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Finite Element Analysis of Stress Evolution in Si based Front and Back Ends Micro Structures

Vincent Senez[a)*], Aldo Armigliato[b)], Giovanni Carlotti[c)], Gianpietro Carnevale[d)], Herve Jaouen[e)] and Ingrid de Wolf[f)]

[a)] IEMN-ISEN, UMR CNRS-8520, Avenue Poincaré, B.P. 69, 59652 Villeneuve d'Ascq Cedex, France
[b)] CNR-IMM, Via P. Gobetti, 101, 40129 Bologna, Italy
[c)] INFM and Dipartimento di Fisica dell'Universita', Via Pascoli, 06123, Perugia, Italy
[d)] STMicroelectronics, via C.Olivetti 2, 20041 Agrate Brianza, Italy
[e)] STMicroelectronics - Central R&D, 850 rue Jean Monnet, 38921 Crolles, France
[f)] IMECvzw, Kapeldreef 75, 3001 Leuven, Belgium

Abstract - **Nowadays, silicon technologies with feature sizes around 100nm are used in the microelectronics industry to produce gigabits integrated circuits. The prime part of numerical simulation in their development is now well established. One of the purpose of the numerical analyses is the improvement of the mechanical reliability. We synthetize in this paper various works we have performed on the macroscopical modeling and simulation of stress problems and their effects in silicon technologies.**

I. INTRODUCTION

The development of silicon technology toward miniaturization leads to the manufacturing of integrated structures exhibiting complex geometry, diversity of materials and very wide ranges of manufacturing conditions. As a result of this evolution, stress related reliability or misoperations are more and more critical in current silicon technologies. That is why guidelines are necessary to alleviate these kind of problems and improve the technologies. Our objective is to provide the process engineers with a tool that allows to study the mechanical optimization of the various steps appearing in advanced microelectronics processes. This tool has to be able to simulate all the steps occurring in a process flow, starting from bare silicon with an initial stress map and calculating/adding at each step the new stress contributions. All kind of stress sources has to be modeled, the mechanical behavior of the materials has to be implemented accurately, taking into account of their temperature and stress dependences. Finally, the stress effects on chemico-physical phenomena have also to be incorporated since they modify the evolution of the stresses. One important point is the extraction of the different parameters appearing in the models. It is fundamental to calibrate most of them for each manufacturing plant. Indeed, with phenomenological models, it is no sense to believe that there is one universal set of parameters valid for all process flows. When the models are defined/implemented and the parameters are calibrated, the next step is to check that the numerical results fit analytical calculations and agree with experimental results. Finally, mechanical analysis of advanced processes can be carried out and modifications of the process flow can be proposed for critical steps in terms of process conditions and/or geometries. In this paper, we describe our modeling approach in section two, then the procedures to extract the mechanical coefficients are described in section three. In section four, we validate our numerical modeling comparing results of numerical simulations against analytical calculations and against local stress measurements obtained by either micro-Raman Spectroscopy (μRS) or Convergent Beam Electron Diffraction (CBED) techniques. Finally, various applications for Front-End of Line (FEOL) and Back-End of Line (BEOL) processes are given in part five.

II. MODELING STRATEGY

In order to shrink the development duration of up-to-date technologies, two- or three-dimensional (2D or 3D) process simulation capabilities are of prime interest. The difficulty in the numerical modelling of silicon technologies arises from the necessity to ensure at one and the same time: i) a wide prediction capability (i.e.: a high modelling accuracy) and ii) a flexible numerical solution. In mechanical analyses, the modelling accuracy requires to take into account all the sources of mechanical failures. It also involves the characterization and calibration of the thermo-mechanical thin film properties as well as the stress effects in various physical phenomena. The efficiency of the numerical implementation concerns its ability to handle real complex topological configurations within reasonable computing time.

A simulation program, IMPACT [1], based on 2D Finite Element (FE) method, has been developed in order to study the evolution of the mechanical stresses/strains during the fabrication of micro-structures (Fig. 1). The last version of this tool includes models for the stress contributions

* *The author is currently with Institute of Industrial Science, University of Tokyo, 4-6-1, Komaba, Meguro-ku, Tokyo, 153-8505, Japan. E-mail: vsenez@iis.u-tokyo.ac.jp*

coming from: i) the temperature change, ii) the thermal growth of material (i.e.: silicon dioxide and silicides), iii) the etching of materials, iv) the deposition processes which create intrinsic stresses, v) the implantation of dopants, and vi) the structural changes of deposited films due to densification, hydration or dehydration, crystallization,...

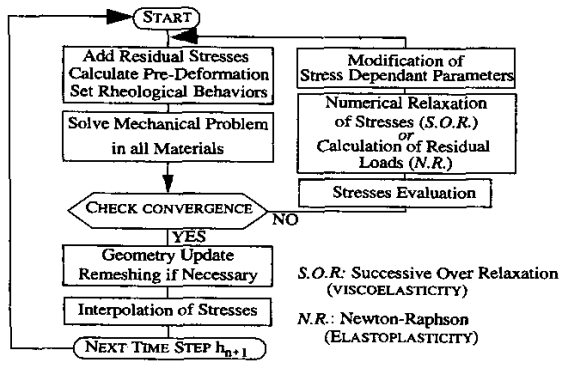

Figure 1: Schematic description of the algorithms implemented in IMPACT to calculate stress/strain evolutions in a silicon micro-structure during its processing.

In the range of temperatures used in the front-end processes ([700°C-1100°C]), and in the range of stresses measured in thin film materials ([20MPa-2GPa]), microelectronics materials show very different mechanical behaviours, from elastic (e.g.: silicon) to viscous (e.g.: higly stressed silicon dioxide at high temperature). Furthermore, at these temperatures and/or stress levels, the amorphous materials may exhibit viscoelastic behaviors and the (poly)-cristalline materials may have elastoplastic behaviors. Simple rheological models have been implemented in IMPACT to represent all of these mechanical properties. The anisotropy of silicon has also been incorporated.

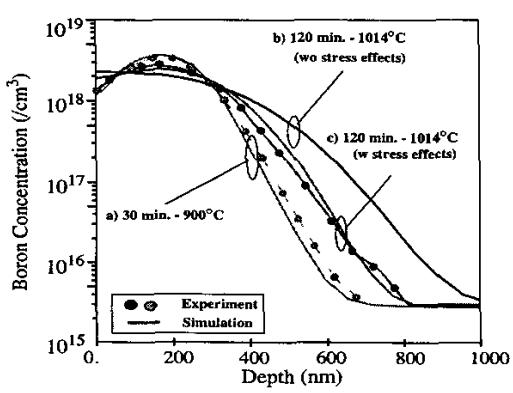

Figure 2: Stress effects on boron diffusion (7.5 $10^{13}/cm^2$) implanted at 70keV and annealed in inert ambient. a) Boron profile after annealing without stresses (bare silicon). b-c) Boron profiles after annealing with stresses induced by 500nm thick nitride layer deposited on top of silicon [2]. Stress effects are implemented in a 5-species diffusion model [3] using the formalism reported in [4].

Concerning the effects of mechanical stresses, the nature of the material, either cristalline or not is an important parameter. In the case of silicon, which has been extensively characterized, we have introduced the effects of stresses on: i) the distribution of point defects, ii) the diffusion of dopants (Fig. 2), iii) the thermal growth of materials. In the case of amorphous and polycristalline materials, stress effects are more difficult to model due to the lack of long range order. However, various properties can also be affected by mechanical stresses. We have introduced stress dependent diffusivity and viscosity for silicon dioxide and titanium silicide.

III. CHARACTERIZATIONS

The mechanical parameters of various I.C. materials currently used in IMPACT have been either taken from the literature or characterized by ourselves. Indeed, for some of them, although studied since several years, one can find lots of discrepancies between the different values reported in the litterature. The explanation comes from the fact that we are using macroscopical law (i.e.: Hooke, Newton, Maxwell,...) for materials deposited in thin films for which small variations of the chemical composition and texture modify largely their mechanical behaviour and for which surface/interface effects become predominant. In our recent studies, we have characterized the behaviors of TEOS (Fig. 3) and HDP silicon dioxides, LPCVD silicon nitride, titanium silicide (Fig. 4) and polysilicon.

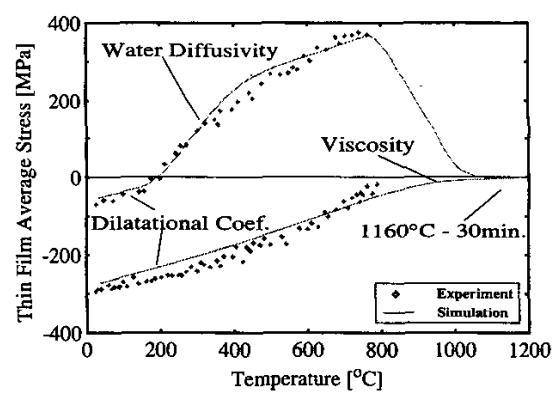

Figure 3: Variation of the average stress during thermal cycling in TEOS oxide film. The numerical simulation corresponds to a cycle up to 1160°C of the as-deposited film. The experiments correspond to the heating up to 800°C of the as-deposited film (first cycle) and the cooling of the annealed film (second cycle). The film thickness is 485 nm.

The different parameters that have been extracted are: i) the Young moduli and Poisson ratios, ii) the viscosities, iii) the intrinsic stress, iv) the thermal expansion coefficient, and v) the volume shrinkage due to densification, water desorption or deshydrogenation. For these physical characterizations, different samples (i.e.: blanket film on silicon wafer) have been prepared by our industrial partners. From these samples, the Young moduli and Poisson ratios have been extracted and the influence of the thickness on

this physical quantities have been studied using the Brillouin Light Scattering (BLS) technique [5]. Indeed, a complete elastic characterization of thin film materials can be successfully achieved using the BLS technique, which relies upon the inelastic scattering of light by thermally activated phonons. This non-conventional technique does not require external generation of acoustic waves and it probes acoustic phonons with wavelength in the submicron range.

These samples have also been used to perform beam bending characterizations. In these experiments, the variation of the curvature of the wafer as a function of the temperature has been measured using laser beam deflection technique. A TENCOR instrument called FLEXUS 2320 have been used. This apparatus allows to perform stress measurements for temperatures up to 900°C. This measurement of the wafer warpage before and after loading allows to determine an uniform value of the mechanical stress induced in thin films using the Stoney formula. These experiments have been simulated with IMPACT and by matching the experimental and calculated stress versus temperature curves, the thermal expansion coefficient and the viscosity of the materials have been extracted (Fig. 3).

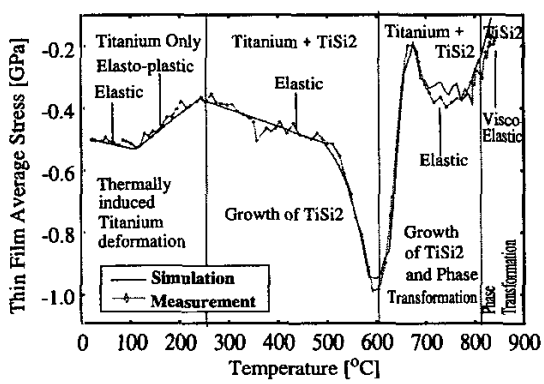

Figure 4: In situ average stress change during the silicidation reaction of Ti/Si with 200nm thick initial titanium layer. The silicidation model is similar to [6] and includes in plane growth and phase transformation.

In the same way, the parameters of the stresses sources have been either taken in the litterature when well known (e.g.: the oxidation/silicidation volume expansion, the volume expansion due to dopant implantation) or characterized by ourselves using different experimental results (e.g.: absorption/desorption of water, deshydrogenation, structural modification) [7]. Finally, the activation volumes of the effects of stresses on material properties when not given by theory have been also calibrated either using empiric calibration method or statistical approach (i.e.: Response Surface Methodology) [8].

IV. VALIDATION

To compare the numerical simulations with the analytical results, we have used the sample model given in insert of Fig. 5 where active regions, 0.22 μm wide, are isolated by 0.48 μm wide shallow trenches. The depth of the trench is 0.35μm. Both analytical and FE calculations were performed in a region which is indicated by the dotted square.

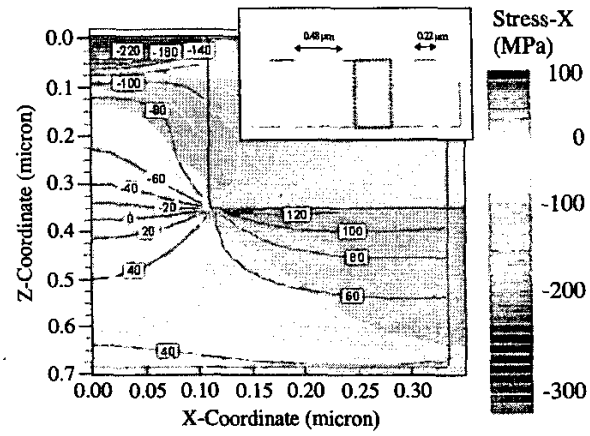

Figure 5: Comparaison of the X stress for the sample given in the insert calculated using 2D analytical model (contours) and FE modeling (surfaces).

The analytical model has been described by Hu [9]. It assumes thermal stress induced by cooling down the sample. A program has been written using the software IGOR to perform the analytical calculations [10]. In order to have a better comparison, we have plotted the results from the analytical model as contours on top of the FE model. Fig. 5 gives the result for the X component of the stress tensor. Altough the contours differ somewhat in shape, the overall correspondence between this simple analytical model and the FE model for plane strain is remarably good for the three components (σ_{zz} and σ_{xz} not shown here).

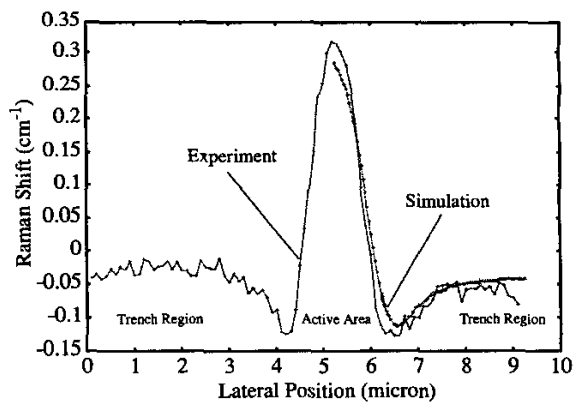

Figure 6: Evolution of the calculated/measured Raman shifts versus the lateral position for a STI structure after densification of the filling materials (TEOS+HDP oxides).

Nowadays, one of the best method for measuring local process-induced mechanical strains in silicon at sub-micron dimensions is μ-RS [11]. Indeed, mechanical strains induce a shift of the Raman peak frequency which can be used as a strain gauge. A μ-RS emulation has been implemented in

IMPACT in order to convert the calculated stress tensors into Raman shifts. Within the european project STREAM [12], the spatial resolution of this technique has been improved reaching about 0.8 μm. It was shown that this spatial resolution can be improved to 0.3 μm when combining an autofocus system with an oil-immersion objective.

Shallow Trench Isolation (STI) structures separated by silicon lines have been used to check the accuracy of the calculations. The STI cell has been processed with a 0.15 micron CMOS NVM technology using TEOS/HDP oxides as filling materials. The entire process has been simulated and the Raman shift has been calculated. The Raman experiments have been performed using the 457.9 nm line of an Argon laser. The sample was positioned under the microscope on an XY-stage and moved in steps of 0.1 μm. At each position a Raman spectrum was measured. Fig. 6 shows the results which are in good agreement in the active and trench regions.

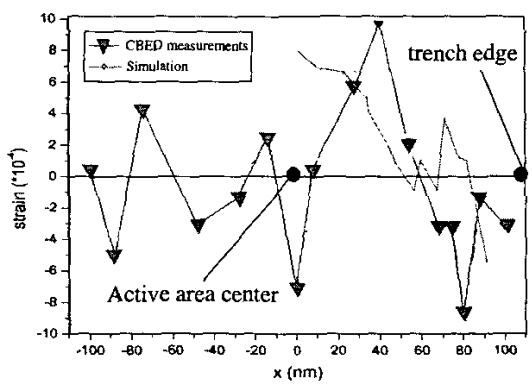

Figure 7: Evolution of the calculated/measured trace of the strain tensor versus the lateral position for a STI structure before densification of the filling material (HDP oxide only).

However, for very advanced CMOS devices, the spatial resolution given by μ-RS is not sufficient. That is why we have used the CBED technique to measure lattice strain in silicon which offers a spatial resolution down to 1 nm. Automated acquisition of CBED patterns via a procedure which can be routinely used by the microelectronics industry has been developped by SIS [13]. A set of points along a 'cut line' in the cross-sectioned structure can be chosen and the electron probe is sequentially located in each of them for the CBED pattern acquisition without requiring the operator's control. Then, the processing of the image, the computation of HOLZ pattern models and strain tensors can be made automatically.

Using this measurement technique, the analysis of the most compact structures (i.e.: length of active area is 0.11μm) has revealed the necessity to use an elasto-plastic model for the rheological behavior of silicon. Fig. 7 shows the evolution of the trace of the strain tensor in the active area obtained by CBED and simulation. The yield stress has been fixed to 1.5GPa (von-Mises criterion). One have to mention that this kind of comparison is extremly difficult to carry out due to the large strain gradient in this structure and the error on the localization of the measurement.

In order to compare the Raman and CBED measurements, the CBED data measured on longer structure (i.e.: length of active area is 2μm) have been converted into Raman shifts.

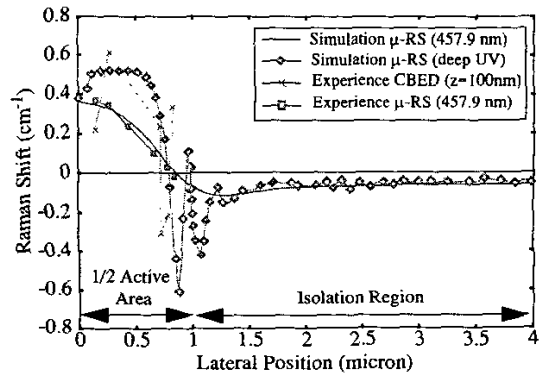

Figure 8: Comparison between the Raman shifts obtained from: 1) simulated μ-RS experiment (457.9 nm), 2) simulated μ-RS experiment (deep UV), 3) CBED experiment (cut line at z=100nm under Si/SiO2 interface), 4) μ-RS experiment (457.9 nm).

We report in Fig. 8 the data corresponding to a sample filled with TEOS/HDP oxides. One can observe discrepancies between these two type of experimental data, in terms of magnitude as well as variation along the X-coordinate. The CBED data show a reduction of the compressive peak in the center of the active area which is not seen by the μ-RS. On the contrary, both measurements exhibit a reduction of the compressive peak towards the border of the active area. The CBED measurements show also a second, smaller, compressive peak at the edge of the active area which is not visible in the μ-RS measurements. After calculation of the Raman shifts from the simulated stress tensors using the features (i.e.: beam diameter and depth of absorption) of a 457.9 nm Argon laser, we have obtained a good agreement with the Raman measurements. If we perform the same calculations but considering an extremly small depth of absorption (100nm) and an extremly small diameter of the laser beam (20 nm), one can observe a better agreement between the Raman shift obtained from the CBED data and the simulations.

V. APPLICATIONS

A 0.15 μm CMOS technology to manufacture Non Volatile Memory (NVM) has been analyzed with IMPACT. This technology uses STI technique to define isolation and active areas. The study focuses on the memory cell process. Fig. 9a shows a typical memory cell layout. First, a tunnel oxide is grown on active area and a first polysilicon layer (poly 1) is deposited and patterned. This layer contitutes the floating gate. After poly 1 definition, an interlayer active dielectric is deposited on top of of the poly 1. The dielectric is called ONO because is made by a triple layer of oxide, nitride, oxide. After ONO deposition, the control gate material is deposited on top of ONO. The process continues with the control gate patterning and the doping of the drain area. After

resist removal, a new lithographic step is done to etch completely field oxide from the source area and to heavily dope the source. After doping, the memory cell is sealed either by oxide deposition (Fig. 9 - samples 1&2) or by thermal oxidation (Fig. 9 - samples 3&4). The spacer and contact formation completes the memory cell. The material for the spacers can be either HTO oxide (Fig. 9 - samples 1&4) or nitride (Fig. 9 - samples 2&3).

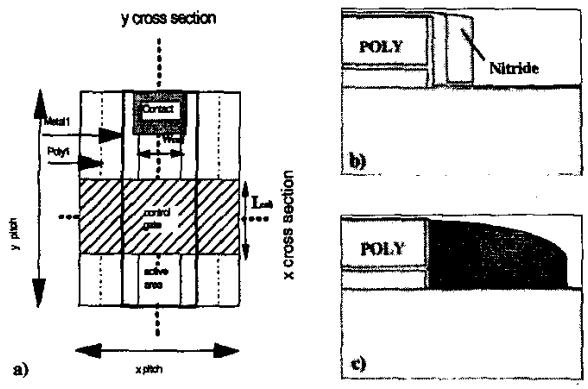

Figure 9: a) Memory cell layout top view. b-c) Simulated morphologies of a NVM cell for different process flows: i) liner deposition + HTO spacer (sample 1), ii) liner deposition + TEOS/Nitride spacer (sample 2), iii) oxidation + TEOS/Nitride spacer (sample 3), iv) oxidation + HTO spacer (sample 4).

The process corresponding to sample 4 (Fig. 9) has been simulated and the results are given in Fig. 10 where one can follow the evolution of the 1D cross section along the x-direction, taken at z=-80nm under the silicon top surface, during the process. After etching of the polysilicon layers, the silicon substrate under the polysilicon gate (active area) is under compression, while there is a slight tension in the source/drain region. The compressive peak is created by the phase transformation of the silicon from amorphous to polycristalline. So, being able to control the crystallization process, one can adjust the residual stress in the active area. Then, the oxidation step generates a Bird's Beak (BB) between the poly 1 and the substrate.

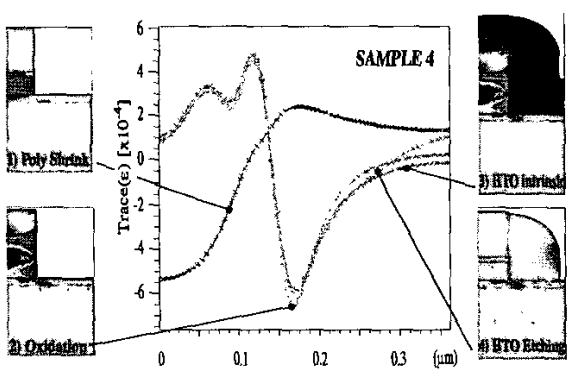

Figure 10: Evolution of the 1D cross section along x-coordinate of the trace of the strain tensor (z=-80nm) during the process flow of the sample 4.

It is well know that this BB induces in silicon a peak of compression at the edge of the mask and a peak of tension at the location where the bending of the mask is maximum. Since the width of the poly line is very small, this peak of tension spreads toward the middle of the active area. As a consequence, the sign of the stress changes in the active area. In the source/drain region the stress reduces slighlty staying positive. After deposition of the HTO layer to form the spacers, the change in the stress/strain map is due to the thermal and intrinsic stress components. One can observe that with the used temperatures and intrinsic stress of HTO, the mechanical stresses do not change so much in the silicon. The next step is the etching of the spacers. In case of HTO, the spacers are quite large and their etching does not strongly modify the state of the stress/strain in the silicon substrate which is finally tensile under the gate, reaches a compressive peak at the edge of the poly line and tends to zero far from the edges of the spacers.

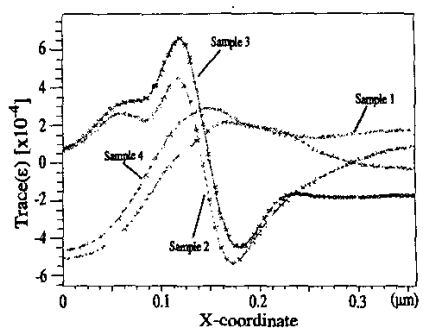

Figure 11: Evolution of the 1D cross section along X-coordinate of the trace of the strain tensor (z=-80nm) at the end of the process flow for the four samples.

In Fig. 11, we have gathered the different results obtained for samples 1-4. The calculations show that the best compromise is obtained by sample 4 which gives at the same time a small tensile stress in the active and source/drain areas. However, with an appropriate stress engineering of the intrinsic stress of the spacers, samples 1&2 would be better, preventing the appearance of the stress peak at the edges of the line.

The second application is the analysis of the BEOL process of a 0.12 µm CMOS technology. The interconnections of the different active areas are obtained with a (1+6) level architecture. The active transistors are sealed with a dielectric layer called the Pre-Metal Dielectric (PMD) in which contacts to active area are formed (Plug). Then a diffusion barrier (TiN) is deposited, followed by tungsten deposition. This stack forms a first Local Interconnection Level (LIL) and contacts. The six subsequent levels are obtained by successive depositions of low-k dielectric (HSQ) and copper. In this study, a TEOS layer has been used and only mechanical behavior of metal 2 is investigated. In the calculations, copper, TEOS and nitride are

deposited at 400°C. It has been shown that the residual stress in the metal 2 line depends more on the geometry than on the process conditions [14]. The influence of the: i) aspect ratio (h/w), 2) line spacing (p), iii) via, and iv) upper level line on the residual stress in metal 2 are reported here. On can observe that for a high aspect ratio (h/w=1.95), the decrease of the line spacing from p/w=10 (Fig. 12a) to p/w=2 (Fig. 12c) increases the X-stress in the copper line. On the contrary, for a small aspect ratio (h/w=0.35), the decrease of the line aspect ratio from p/w=4 (Fig. 12d) to p/w=1.18 (Fig. 12b) has almost no effect on the X-stress of the line. One can also see that line with high aspect ratio (h/w=1.95) has higher X-stress than line with small aspect ratio. Decreasing the spacing increase the tensile X-stress in the dielectric between the line up to 325MPa (Fig. 12b-c). Here the calculation are performed with TEOS oxide. It is expected that with low-k dielectric, having small elastic constants, this tensile state could largely increases and could generates crack during the deposition of the nitride layer. The calculations show also that the X-stress in metal 2 is not modified by the addition of a metal 3 line (Fig. 12e) whatever the aspect ratio and spacing. Finally, the effect of a via depends on the width of the line. If the via has the same width, the average X-stress of the line decreases but the peak value does not change. On the contrary, if the via is narrower than the line (Fig. 12f), it tends to increase the peak value and to increase shear stress.

VI. CONCLUSIONS

A overview of stress modeling and simulation for advanced silicon technologies has been given. Our recent work on this topic has focused on the calibration of mechanical models and their application to FEOL and BEOL of very advanced CMOS technologies. It has been shown: i) the capability of the CBED technique to analyze very finely the strain state of microelectronics structures, ii) the limitations of Raman technique to show up sharp strain gradients present in extremly compact microelectronics structures, and iii) the good predictivity of the stress models available in IMPACT. The next step lies in establishing a direct link between the stress state obtained by process simulation and incorporation of this state in electrical (device) simulation.

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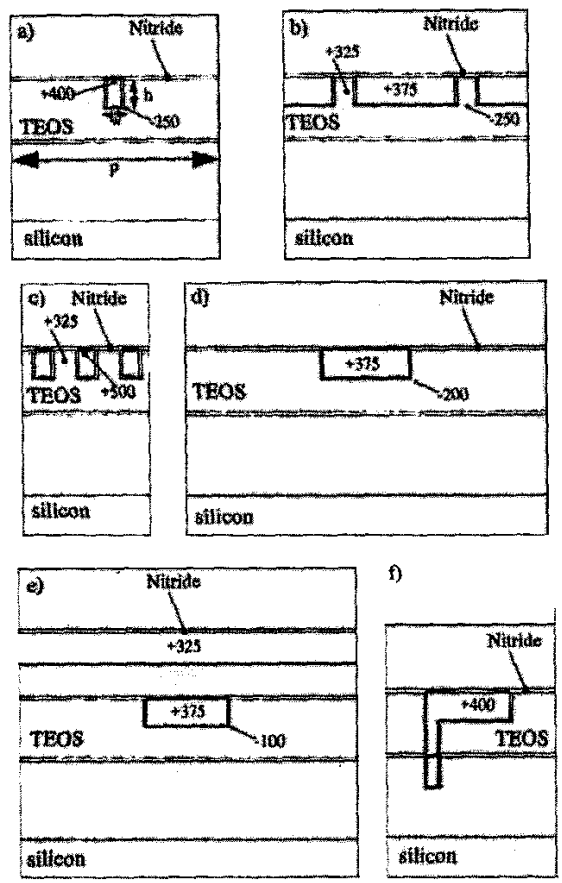

Figure 12: X-Stress map for various layout of the interconnects network: a) large aspect ratio, large spacing, b) small aspect ratio, small spacing, c) large aspect ratio, small spacing, d) small aspect ratio, large spacing, e) small aspect ratio, large spacing, upper level line , f) small aspect ratio, small spacing and via to level 1.