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Analysis of injection current with electron temperature for High-K gate stacks

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Abstract – **Though, high dielectric constant material is a possible near future candidate to suppress gate current densities of MOSFETs, the barrier height generally decreases with increasing dielectric constant. In this paper, the injection current through gate stacks has been calculated while taking into account the electron temperature using the W.K.B. method to understand the impact of the injection current from the drain edge.**

1. Introduction

High dielectric constant (high-K) material is a possible near future candidate to suppress gate (injection) current densities of MOSFETs. The suppression of gate current densities is a critical issue not only on the power consumption at Vg = 0, but also on the reliability problem at Vg = Vdd. Furthermore, in the case of low stand-by power transistors, the allowable leakage current densities are limited by battery life at any gate bias condition. In previous studies, stacks with SiO2 or oxy-nitrides between silicon and high-K dielectrics have been recommended to be formed solely to prevent the mobility degradation due to the low carrier mobility at the interface between the silicon and high-K dielectrics. However, near the drain edge, the population of the high-energy electrons increases with the decreasing channel length of MOSFETs. It is known that the injection probability increases with electron energy, and the barrier height generally decreases with increasing dielectric constant. Also, the rate of injection into dielectric increases with the decreasing barrier height. Consequently, injection current densities in gate stacks from the drain edge will exceed those from the source edge. In previous studies, the measurements [1] have been obtained only for long channel devices, and calculations [2] have not included the electron energy enhancement.

In this paper, to understand the impact of the injection current from the drain edge, the injection current through gate stacks has been calculated including the electron temperature, for the first time. The W.K.B. method [3] is used to calculate the injection probability including direct / Fowler-Nordhiem tunneling and thermoionic emission. Also, a new design criterion for gate stacks is proposed based on our calculation results.

2. Injection model

The injection current density is expressed as follows,

$$J = \int_{E\,\min}^{\infty} dEx\left(\frac{8q\pi m_1 kT_1}{h^3}\ln\{1+\exp[(E_{f1}-E_x)/kT_1]\}\right. \\ \left. -\frac{8q\pi m_3 kT_3}{h^3}\ln\{1+\exp[(E_{f3}-E_x)/kT_3]\}\right)\tau(Ex) \quad (1)$$

Where m_1, m_3 are the effective mass of the silicon 1 and silicon 3, respectively, as shown in the Fig.1. T_1, T_3 are the electron temperature, and E_{min}= max(E_{c1}, E_{c3}), where E_{c1}, E_{c3} are the conduction band energy and E_{f1}, E_{f3} are the Fermi level, of the silicon 1 and 3,

respectively. And x is the direction normal to the interface and E_x is energy component of the electron in the x direction.

The injection probability of stack $\tau(E_x)$ is calculated by the W.K.B. method, and when $\tau(E_x)$ is small, $T(E_x)^{-2}$ is calculated approximately from the product of the injection probability of each region as follows,

$$\tau(E_x) = \{2T(E_x)^2 + \frac{1}{8}T(E_x)^{-2}\}^{-1} \quad (2)$$

$$T(E_x)^{-2} = \prod_{i=1}^{n} T_{(i)}(E_x)^{-2} \quad (3)$$

$$T_{(i)}(Ex)^{-2} = \exp[-2\int_{l_{i-1}}^{l_i} k_{2(i)}(x')dx'] \quad (4)$$

$$k_{2(i)}(x) = \sqrt{\frac{2m_{ox(i)}(x)}{\hbar}(V_{2(i)}(x) - E_x)} \quad (5).$$

Where, (i) indicates the index of stack regions, and n is the number of stack regions (in this paper, n = 2). And, $k_{2(i)}$ is the wave number of the Schroedinger function represented by the potential $V_{2(i)}$ and E_x.

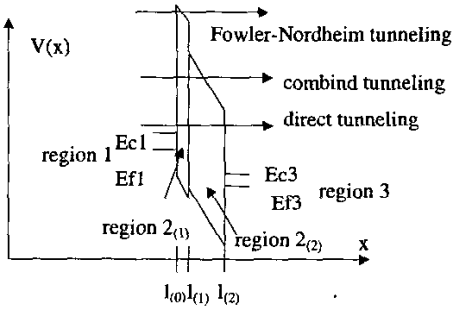


Fig.1. The band structure along the electron injection path.

3. Calculation Results

The calculated points in the device structure are shown in Fig.2, where ΔV is the potential difference applied to the dielectric between the gate poly-silicon and the substrate silicon. The calculated results for ΔV = 1 V correspond to injection current densities from the source region to the gate region. The calculated results for ΔV = 0 V are correspond to injection current densities from the drain region to the gate region.

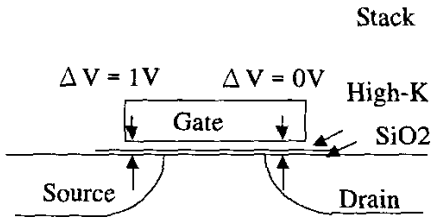


Fig.2. The calculated bias condition and device structure.

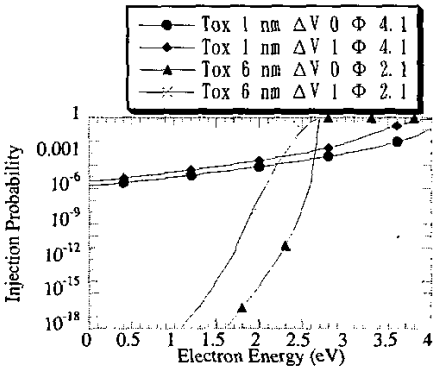


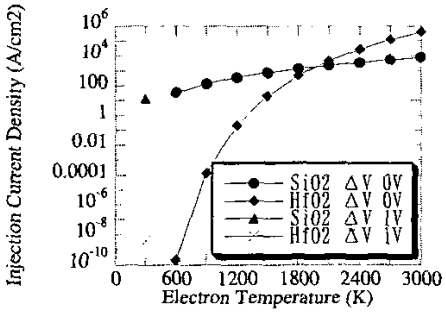
Fig.3. The calculated electron energy dependence of the injection probability for SiO2 ($\mathcal{E}$ 3.9, Φ 4.1 eV, m* 0.41 m_0) and high-K dielectric (HfO2) ($\mathcal{E}$ 23.4, Φ 2.1 eV, m* 0.2 m_0) with ΔV = 0 V and ΔV = 1 V (300 K). EOT is 1 nm.

The calculated electron energy dependence of the injection probability is shown in Fig.3. The relative dielectric constant $\mathcal{E}$ = 23.4 and the barrier height Φ = 2.1 eV for HfO2 [1][4] are used in this calculation. Injection current densities through Equivalent Oxide Thicknesses (EOT) of 1 nm are calculated. As shown in Fig.3, the injection probabilities increase with ΔV, and the injection

probability of HfO2 is very small in low energy compared with those of SiO2, but increases rapidly with electron energy and exceed those of SiO2 because of the low barrier height.

The electron temperature dependence of the injection current densities in the device structure shown in Fig.2 are shown in Fig.4 for SiO2 and high-K dielectric (HfO2 is used as a typical example). In the calculation, the electron density at the gate poly-silicon is 10^{20} cm^{-3} at a temperature of 300 K. The electron density at substrate silicon near surface is 10^{20} cm^{-3} at a temperature of 300 K (ΔV = 1 V which corresponds to injection current densities from the source region) or at various temperatures (ΔV = 0 V which corresponds to injection current densities from the drain region).

As shown in Fig.4, the injection current densities, where ΔV = 0 V, increase with Te (electron temperature) and those above 600 K are larger than those where ΔV = 1 V at 300K with corresponding regions. The injection current densities through HfO2 where ΔV = 0 V at high temperatures (i.e., Te is above 2100 K) are larger than those through SiO2 with corresponding temperatures.



Fg.4. The electron temperature dependence of the injection current densities for and high-K dielectric (HfO2) with ΔV = 0 V and ΔV = 1 V (300 K). EOT is 1 nm.

In Fig.5, the ratio dependence of high-K dielectric in the gate stack structure on the injection current densities through the dielectric stacks are shown. As an example, a ratio of 0.2 means 0.8 nm SiO2 on Si substrate and 1.2 nm (EOT 0.2 nm) of high-K dielectric above (total EOT is 1 nm). The left side of the figure (high-K ratio = 0) is the values for pure SiO2, while the right side (high-K ratio = 1) represents pure high-K dielectric. The injection current density decreases with the high-K ratio at the lower electron temperature; however at higher electron temperatures, the injection current density begins to rise for increasing higher ratio values due to the increase of the high-energy electrons. Thus, Fig.5 shows the necessity with a 0.4-0.6 nm thickness for SiO2 under high-K dielectric in a stack with 1 nm EOT, to suppress the injection current near the drain edge.

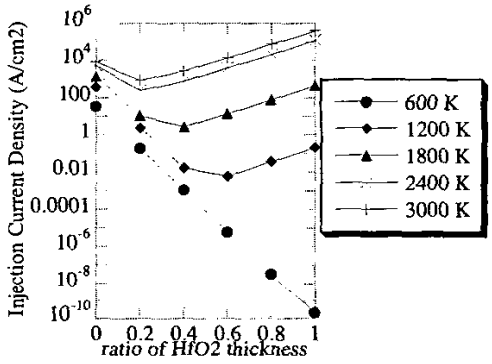


Fig.5. The ratio dependence of high-K dielectric of the gate stack structure on the injection current densities with an EOT of 1 nm for different electron temperatures of the substrate silicon surface. ΔV = 0V.

In Fig.6, the electron temperature dependences of injection current density with different barrier heights are shown to illustrate the effect of lowering the barrier height. The injection current density dramatically increases with decreasing barrier height. Consequently, barrier height is shown to be a critical parameter for carrier injection.

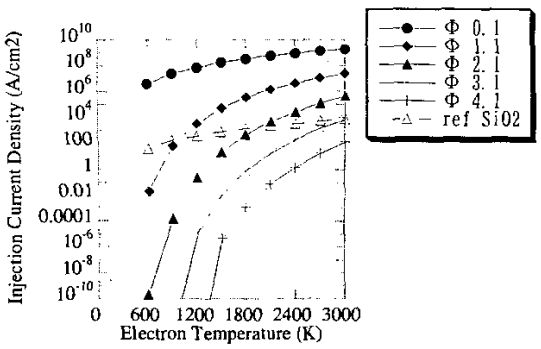


Fig.6. The electron temperature dependence of injection current densities with respect to different barrier heights for high-K dielectric (ε 23.4, m* 0.2 m_0) and SiO2 shown as a reference. EOT is 1 nm. Δ V = 0V.

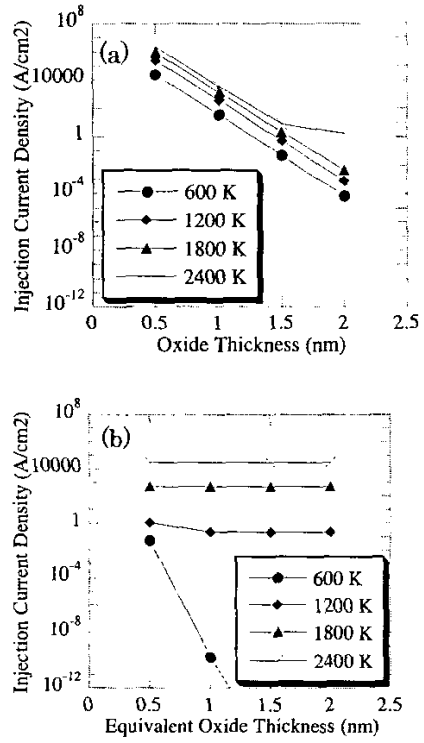


Fig.7. The equivalent oxide thickness (EOT) dependence of injection current densities through (a) SiO2 and (b) high-K dielectric. Δ V = 0V.

In Fig.7, the EOT dependence of injection current densities through SiO2 and of high-K dielectric values are shown. As shown in Fig. 7, the injection current densities through SiO2 are strongly dependent on the EOT value. However, the injection current densities through of high-K dielectric show negligible dependence on the EOT when the electron temperature is higher than 1200 K. Therefore, a stack structure incorporating some thickness of SiO2 is indispensable in the suppression of the injection current for EOT values of approximately 1 nm or more.

4. Conclusions

The gate injection current densities through different high-K dielectrics have been investigated by the W.K.B method taking into account the electron temperature. The gate injection current increases with the electron temperature (especially through high-K dielectric) as the barrier height of high-K dielectric is much lower than that of SiO2. Although in previous studies, the stacks with SiO2 or oxy-nitrides between silicon and high-K dielectrics have been recommended to be formed as thin as possible, our results indicate for the first time the necessity of some oxide to suppress injection current densities generated from high-energy carriers generated near the drain edge. It is thus proposed that the optimized stack structure should contain some SiO2 (or oxy-nitride), to suppress the injection of high-energy carriers. We anticipate that our results will also be applicable to the design of an optimized stack structure using other dielectrics.

Refarences

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[2] S. Mudanai et al., IEEE Trans Electron Devices, 47, p. 1851, 2000.

[3] J. P. Shiely, "Simulation of Tunneling in MOS Devices", Ph. D. Dissertation, Duke University, 1999.

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