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Technology Modeling for Emerging SOI Devices

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Abstract – New physical models, algorithms, and parameters are needed to accurately model emerging silicon-on-insulator (SOI) devices. The modeling approaches for various SOI technologies are discussed in this paper.

FRONT-END TECHNOLOGY MODELING

Technology Modeling has played an important role to CMOS technology research, development, and manufacturing. A typical technology computer-aided-design (TCAD) tool set includes process simulator, device simulator, and user environment. For process simulations, we rely on vendor-supported platform with proprietary physical models and calibration methodology. An extensive, detailed physical model set for oxidation, diffusion, deposition, etching, and implantation are needed to model accurately the full CMOS process flow [1]. IBM has a long history in device modeling. In the early 1990, IBM consolidated all the internal device simulation tools. The Fielday program was selected as the standard semiconductor device simulator. E. Buturla and P. Cottrel first wrote Fielday. It was then re-written, in 1987, by J. Johnson and S. Furkay to introduce better gridding and three-dimensional capabilities [2]. Many features [3-4] were subsequently added to the program (Fielday-II). In 1996, M. Ieong initiated a re-architecture project for the Fielday program. Emerging software technologies such as object-orientation and scripting languages were introduced into the top level of the code. New physical models and numerical algorithms are added to address critical issues in DRAM and CMOS logic technologies. The FIELDAY-III features 1) mixed-mode coupled device-circuit simulation capability, 2) improved physical models including quantum correction model, mobility model, and Schottky tunneling contact model, 3) advanced computational algorithms and efficient memory utilization. IBM's user environment (NISE) was written by S. Fischer in 1995, and includes optimized job farming algorithms, a GUI environment for standard TCAD operations, and a scripting environment supporting less standardized TCAD automation tasks [1]

II. SILICON-ON-INSULATOR

The SOI CMOS technology is becoming mainstream for high-performance logic applications due to its performance gain over bulk CMOS [5]. The main difference in SOI CMOS is that the transistors are built on top of a SOI substrate. A schematic SOI MOSFET structure is shown in Figure 1. The buried-oxide in SOI can effectively reduce the junction capacitance. It also eliminates the so-called reverse body effect in stacked circuits. As a result, SOI technology offers faster circuit and consumes less power. A more detailed description of SOI technology can be found in [6] and [7]. Technology modeling is an integral part of the SOI CMOS technology development. Selected examples are discussed in the following subsections.

II.A. PROCESS MODELING IN SOI

Predictive capability for a different technology generations necessitates 1) updated implant tables; 2) transient enhanced diffusion model considering interaction between dopants, interstitials, and vacancies (three-stream TED model); 3) accumulated damage from multiple implants (Plus-x damage model); 4) Amorphization due to implant damage; 5) Transient activation and deactivation of dopants; 6) Dislocation loops as source and sink for interstitials; 7) three-phase segregation model. The complexity of process models increases rapidly for advanced technology. Model calibration with experimental data is the most important step for successful process simulations. The existence of buried oxide in SOI substrate can altered the dopant diffusion in the SOI layer. Extensive experiments and calibration [8] were conducted to better model the dopant diffusion in SOI layer.

II.B. JUNCTION LEAKAGE

The floating –body-effect is a unique characteristic in SOI MOSFET. Better understanding of such effect is crucial for overall chip performance [9]. Because of the power supply voltage scaling and strong halo used in scaled MOSFETs, the body potential in a partially-depleted-SOI MOSFET at and below threshold can be characterized by two back-to-back diodes [10]. The body potential at off condition can be estimated from the forward and reversed diode characteristics of the Source/drain to body junctions

(see Figure 2). A weak temperature dependence of diode current at high reverse bias suggests that leakage is dominated by band-to-band tunneling. At low bias, the leakage current is dependent on the trap density related to defects. This leakage can be accurately described by a field-enhanced carrier lifetime model in a SRH-like recombination formulation. However, the defect density is highly process dependent. The ion-implantation species and its implant energy and rapid thermal anneal (RTA) conditions can substantially affect the defect related leakage current. Reducing the junction area can substantially increase the floating body effect. Diode characteristics from a body-tied SOI MOSFET at different temperatures are needed to separate the defect-related current and the band-to-band tunneling current. Special attention must be paid to ensure that diode current is not obscured by the gate induced drain leakage (GIDL). The formulations for junction leakage can be described by the models proposed by Hurkx [11] and Kane [12].

II.C. SOFT-ERROR-RATE

Soft errors in memories have been a known serious problem since the 1970's [13-14]. Scaling of devices has only caused the soft error rate (SER) susceptibility of memories as well as random logic to increase due to 1) smaller charge storage capability and 2) reduced supply voltage causing smaller margins for noise currents. Low energy cosmic rays, which have caused negligible SER in the past, are now causing more havoc as devices are scaled. Error correction codes and/or redundancy have been implemented on-chip and at a system level to counteract the deleterious effects of soft errors. IBM has a full suite of tools to analyze the SER of a given technology. Process modeling is done with Tsuprem4 to obtain accurate doping profiles. Fielday is used to simulate the charge collection process in devices [15]. Figure 3 shows results of calculations done to calibrate the model used for electron-hole pair generation due to energetic particles used in Fielday [16]. Circuit simulations are then performed using AS/X models and a circuit description from layout information. Physical understanding from this modeling is then used in the soft error Monte Carlo modeling program SEMM [17] to calculate the SER of a given circuit. Because of the floating body effect in SOI devices, we have recently implemented a new model for charge collection within SEMM to accurately model the SER of SOI devices [18]. Figure 4 and 5 shows that silicon thinning is an effective method to reduce the SER of SOI devices.

III. EMERGING SOI TECHNOLOGY

The exponential grow of microelectronics industry is mainly attributed by the successful CMOS scaling in the past three decades. The searches for higher performance together with severe competition have driven CMOS scaling to ever-increasing rate. New device structures and new materials will likely be needed to maintain the performance trend. The 2001 ITRS roadmap [19] have identified the ultra-thin body SOI, the band-engineer transistors, and the double-gate MOSFETs as the most promising candidates to extend the limits of conventional CMOS scaling. Both the industry and the academia are actively conducting research in these emerging devices. However, the models and parameters in existing TCAD tools are often insufficient for such advanced devices and materials. We will discuss our experiences in modeling these emerging devices in the following subsections.

III.A STRAINED-SILICON CMOS MODELING

Strained silicon device (see Figure 6) is an attractive band-engineering transistor. It can increase CMOS drive current in addition to the improvements by geometric scaling. Biaxial tension (See Figure 7) in the silicon channel improves carrier mobility in both n-FET and p-FET by up to 80% [20]There are many options for modeling strained silicon CMOS devices with Fielday. One option is to use 2D process simulations (Tsuprem4) to calculate the stress/strain in silicon. Models for the effect of local stress and strain on bandgap and mobility can then be included [21]. Another choice, which is typically used for SiGe base HBT simulation, is to read the local Ge content into Fielday. Band offsets as a function of Ge mole fraction are then used to locally vary the conduction and valence band edges [22]. A third option that seems to work well for strained silicon on unstrained $Si_{1-x}Ge_x$ is to define a local value of conduction and valence band offset for the structure. Mobility model parameters have then been calibrated to hardware so that SSCMOS devices can be simulated with Fielday [23]. Because the conduction band edge is lowered for strained silicon NMOS devices, compared to conventional silicon devices, a typical design point for strained silicon devices would have better than 50% improvement in performance due to mobility enhancement and reduced short channel effect. Dopant diffusion in strained silicon and SiGe are drastically different. Boron diffusion is retarded in SiGe while Arsenic diffusion is enhanced [24]. Since junction engineering is one of the most important part in device design, the

dopant diffusion in strained silicon must be accurately modeled to provide proper design guidance.

III.B. ULTRA-THIN BODY MOSFETS

In conventional CMOS scaling, the oxide thickness, junction depth, and depletion width are scaled to support gate-length scaling. The accelerated scaling has pushed the gate-dielectric and junction technology to near its physical limits. Ultra-thin body SOI is a promising device option to continue CMOS scaling without deviate too much from conventional planar CMOS devic es [25-26]. Interesting physics can be observed when the SOI thickness, Tsi, is scaled to thinner than inversion layer in bulk CMOS [27]. The channel capacitance is increased with decreasing Tsi. More electrons are occupied in the lower effective-mass band as Tsi is scaled. The peak of the inversion charge distribution is moved closer to the interface with lower effective mass, which in turn increases the gate-to-channel capacitance. This phenomenon cannot be predicted with simple quantum correction algorithms [28-29]. Coupled Schrödinger-Poisson equations must be solved to obtain the sub-band information. In ultra-thin body device, the phonon-limited electron mobility is degraded as Tsi is scaled. However, at a certain range of Tsi, the electron mobility could be enhanced by a higher populated 2fold valley, which has lighter effective mass. The mobility is degraded again as Tsi is further scaled. The coulomb scattering from the back-gate interface and the surface roughness scattering could degrade the carrier mobility. Due to the complexity of the band structure, hole mobility in ultra-thin silicon is much more complicated. Reliable experimental data and theoretical calculations are still lacking.

III.C. DOUBLE-GATE MOSFETS

Double-gate (DG) device (Figure 8-9) is the most promising candidate for ultimate CMOS scaling [30-31]. Excellent short-channel-effect control, higher low-field mobility, and near ideal subthreshold slope are the major advantages for double-gate devices. Recent reported experimental data are very promising. Double-gate device performance that can rival conventional CMOS has been realized [32-33]. The SER for double gate devices is expected to be quite good [18] because of many factors. 1) Because the width of a DG device can be approxima tely half that of a conventional SOI device, there will be few particles that can generate charge in regions sensitive to charge collection. 2) Typical DG designs use ultra-thin silicon, which by itself has been shown to improve the SER. and 3) A fully depleted DG device would show no additional charge collection due to parasitic bipolar effects, typically seen in partially depleted SOI designs. Fig. 5 compares the expected alpha particle induced SER that was calculated using SEMM for various DG designs. We expect a one order of magnitude improvement in SER compared to a conventional SOI device if a relatively thick silicon layer of 50nm is used. Thinning the silicon further to 20nm should provide another order of magnitude improvement in SER.

III.D. SCHOTTKY SOURCE/DRAIN MOSFETS

External resistance is becoming more and more important in scaled CMOS technology. It could degrade the performance of CMOS substantially. In theory, replacing the source/drain by metal-silicide can reduce the external resistance. It could also improve the short-channel-effect because of more abrupt junctions and better off current control by the Schottky barrier. A realistic, physical tunneling contact model in a CAD-based device simulator is needed to evaluate such devices [34]. The tunneling current through the barrier can be converted into a local generation/recombination process where the local rate depends on the local Fermi-level and the potential along the tunneling path. This is possible because the tunneling integral over distance and energy can be transformed into a double integral over distance. For each contact node, a tunneling path is extracted from the 2D/3D spatial domain using a carefully constructed mesh. One application of this model shows that neither lumped contact resistance nor distributed contact resistance can accurately describe current flow into realistic silicide regions [35]. Because of the total elimination of Source/Drain regions, the Schottky S/D FETs have the advantage of lower sheet resistance and potentially higher density. However, the contact resistance associated with the finite Schottky barrier is too high. A lower barrier height material should be used to minimize the contact resistance. In practice, not many low-barrier height silicide materials are available. In fact, a negative barrier material must be used in order to achieve enough thermal injection for high-saturated current. An interesting approach is to combine the Schottky source/drain and ultra-thin body devices [36].

IV. VARIATIONS

Variations in MOSFET are an increasingly important problem as device dimensions shrink. Threshold voltage variation due to fluctuation in number and position of dopant atoms has received increas ing

attention. Three-dimensional device simulations are the most accurate approach to study this phenomenon [37]. D. Frank reported a program [38] that can analyze doping fluctuation effects for arbitrary doping profiles. Every Silicon atom site in the entire device simulation volume is associated with a random number. For each atom, the random number is compared against the local probability of a dopant atom to decide whether that atom is a dopant. These dopants are then interpolated back to the simulation grid [38]. Asenov *et al* [39] reported that quantum confinement could add another 24% to the uncertainties. Line width variation is another important issue in small-scaled devices. The roughness on the edge of the line does not scaled as the line-width is scaled. A fast method using multiple-2D device simulations to study line-edge roughness effect was reported [40]. It was concluded that the line-edge-roughness effect could cause even more variations in device performance compared to the dopant fluctuation effect. For ultra-thin body SOI single-gate and double-gate MOSFETs, the variation in SOI thickness will likely become the major source of variations. In addition to threshold voltage variations, the capacitance and mobility are also affected by the SOI thickness. More experimental and theoretical works are needed for such emerging SOI devices.

V. CONCLUSION

We have discussed key modeling tools and methodologies used to support research, development, and manufacturing of emerging SOI device technology. Although commercial TCAD tools are available, new physical models, parameters, and algorithms are needed to study these novel device structures.

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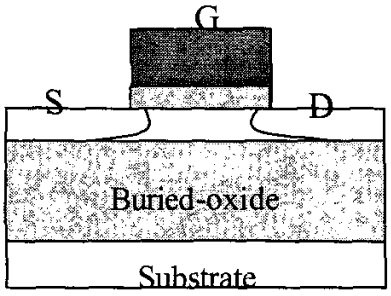

Figure 1: SOI device schematic

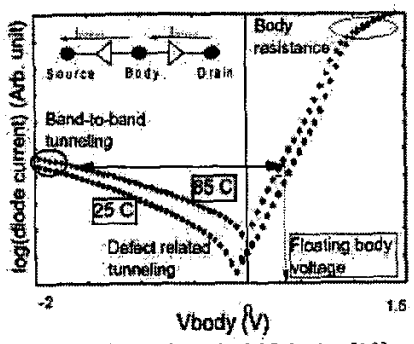

Figure 2: Junction leakage in SOI device [10]

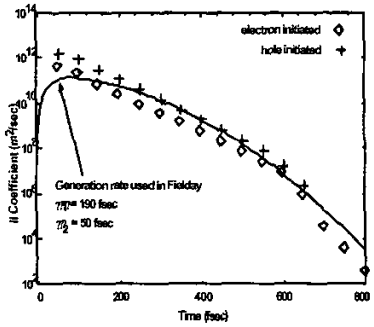

Figure 3: Electron and hole impact ionization coefficients.

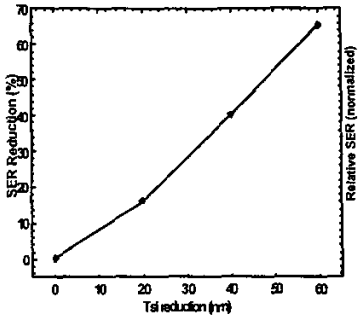

Figure 4: Effect of silicon thinning on alpha-particle induced SER.

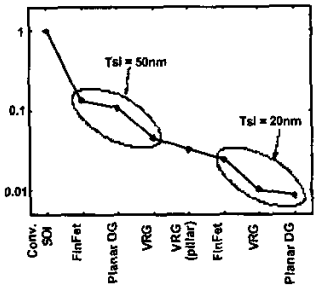

Figure 5: Expected SER reduction in various DG structures [18].

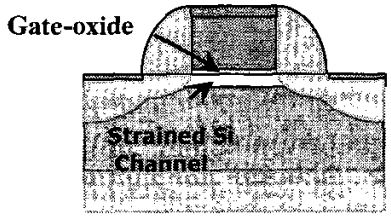

Figure 6:Strained-silicon device schematic

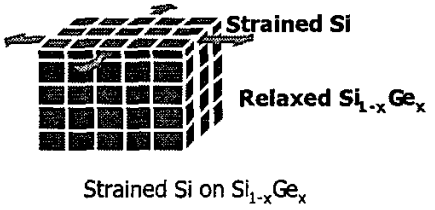

Figure 7:Strained can be generated by lattice mismatch.

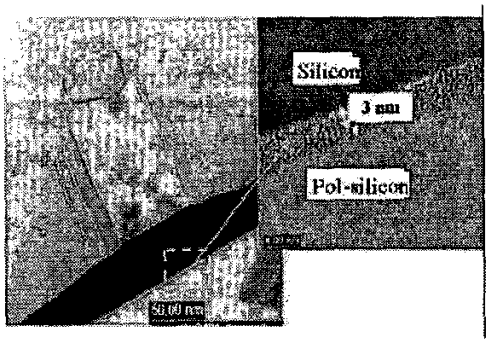

Figure 8:Planar double-gate SOI device [32]

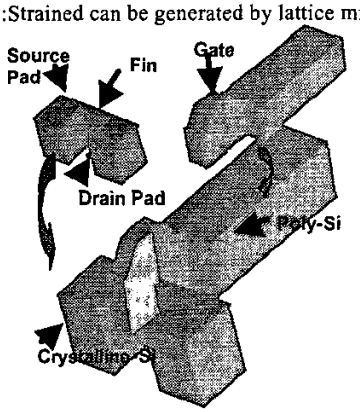

Figure 9:FinFET double-gate device [33]