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A New Non-Pair Diffusion Based Dopant Pile-Up Model for Process Designers and Its Prediction Accuracy

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Abstract – **This paper describes an effective model which reproduces the dopant pile-up in the Si/SiO2 interface using a conventional process simulator that solves one equation for each impurity. The proposed model is based on the physics where the key factor of RSCE is the dopant pile-up in the Si/SiO2 interface. The capability of the model is investigated though the comparison to measurements in actual fabricated nMOSFETs for different process technologies.**

I. INTRODUCTION

A short-term optimization of device performance using TCAD has been required for the design of advanced devices. Since we have to run simulations many times for device optimization, statistical analysis, and calibration, the reduction of the calculation time and total number of parameters is very important. Although the pair diffusion model [1] deals with physical phenomena precisely, the calculation time and total number of parameters increase. For the most of process designers, the use of the simple model which reproduces the dependence of various processes for reverse short channel effect (RSCE) by a few physical parameters is desirable for the prediction of electric characteristics in next trial fabrication. The model has to ensure the simulation accuracy in the local process window, and also have a capability of speedy calculation.

In this paper, we propose an effective model which reproduces the RSCE for various processes by a few parameters. The purpose of the model is that TCAD provides high performance for a short-term device optimization. The capability of our model is investigated through the comparison to measurements in actual fabricated nMOSFETs for different process technologies.

II. PROPOSED MODEL

According to pair diffusion model [1], general dopant flux relation with point defects ($D_{BI}\nabla[BI]$) consists of the channel dopants broadened by the enhanced interstitials ($\propto D_{BI}(I)\nabla[B]$) and the dopant pile-up at the Si/SiO2 interface due to gradient of excess interstitials ($\propto D_{BI}(B)\nabla[I]$). We assume that the dopant pile-up is formed by diffusing dopants into the interface from the substrate without repeating connection and separation of pairs (BI) for time length which can ignore their reactions.

Schematic explanation of our model is shown in fig.1. The amount of the pile up on one cell at the interface, $C_{int}(x)$, is calculated by integrating the component of the dopant diffusion, $\Delta C(x,y)$, on each cell in the substrate

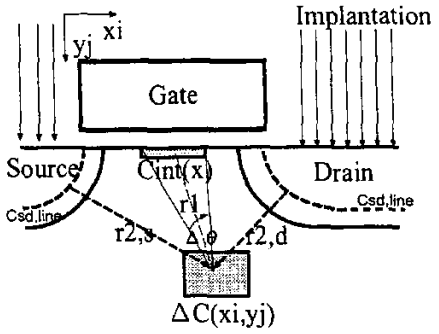

Fig.1 Conceptual diagram of the proposed model

which separates from the location of the pile up with the distance ($r1$). $C_{int}(x)$ is written as follows:

$$C_{int}(x) = \sum_{i}^{ni}\sum_{j}^{nj} \Delta C(x_i, y_j) \tag{1}$$

$$\Delta C(x_i, y_j) = A \times \frac{C_{sd,peak}}{C_{sd,line}} P_b \times P_i \times P_r \times C(x_i, y_j) \tag{2}$$

$$P_b = \exp\left(-\frac{r_1}{\lambda_1}\right) \tag{3}$$

$$P_r = \exp\left(\frac{\Delta\theta}{2\pi}\right) \tag{4}$$

$$P_i = \exp\left(-\frac{r_{2,d}}{\lambda_{2,d}}\right) + \exp\left(-\frac{r_{2,s}}{\lambda_{2,s}}\right) \tag{5}$$

$$\lambda_{2,d} = \left|\frac{r_{2x,d}}{r_{2,d}}\right|\lambda_{2x} + \left|\frac{r_{2y,d}}{r_{2,d}}\right|\lambda_{2y} \tag{6}$$

$$\lambda_{2,s} = \left|\frac{r_{2x,s}}{r_{2,s}}\right|\lambda_{2x} + \left|\frac{r_{2y,s}}{r_{2,s}}\right|\lambda_{2y} \tag{7}$$

where $C(x,y)$, $C_{sd,peak}$, $C_{sd,line}$, and A represent the dopant concentration at the location (x,y), the peak concentration of the S/D region, the line value of an equivalent concentration of the S/D region (e.g., 10^{19} cm^{-3}), and the constant, respectively. $\Delta C(x,y)$ is determined as a function of three probabilities; arrival from the substrate to the interface (P_b), solid angle between the interface and the substrate cells (P_r), and contribution of point defects on S/D region which are caused by implantation damage (P_i). The pile up calculation is repeated until the time length for TED [2]. After that, the conventional Fair diffusion equations [3] are solved.

III. DEPENDENCE ON PARAMETERS FOR DOPANT PILE-UP

To prove the physical validity of our model, the

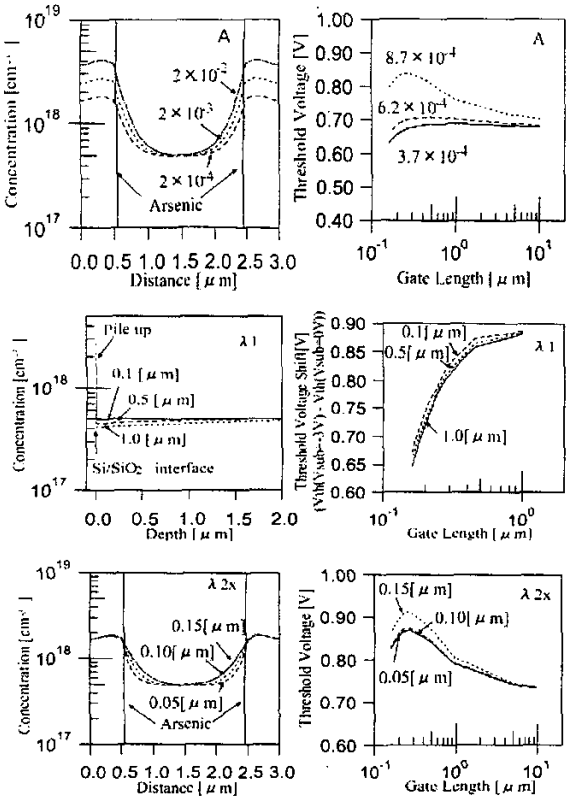

Fig.2 Dependence on parameters for dopant pile-up

dependence on parameters for dopant pile-up is checked for nMOSFETs with constant channel profile (Fig.2). The total number of parameters are four (A, $\lambda 1$, $\lambda 2x$, and $\lambda 2y$). A represents the magnitude of dopant pile-up. $\lambda 1$ relates to the distance from the interface to the substrate where dopant diffusion contributes to the pile up at the interface. $\lambda 2x$ and $\lambda 2y$ correspond to x and y component of the diffusion of point defects from the source /drain (S/D) to the substrate. A, $\lambda 1$, and $\lambda 2x$ can be used to adjust the magnitude, back-bias dependence, and gradient of RSCE, respectively. Calculating the subsequent diffusion equation with time step (Δt) forms the distribution of dopant pile-up in the depth direction. As a result, the calibration strategy of these parameters for electrical chafacteristics is clarified.

IV. APPLICATIONS

The usefulness of the present method is confirmed through the calibration of RSCE of fabricated nMOSFETs for two different process technologies. Fig.3 shows process flows for technologies 1 and 2. To eliminate gate depletion and quantum effect, we use a thick gate oxide. Figs.4 and 5 show the final electrical characteristics for two technologies, respectively. Final parameter sets are listed in table 1. Simulations are in good agreement with experiments for both technologies 1 and 2.

We also check the prediction accuracy of the dopant profiles. Figs.6 and 7 show the simulated dopant

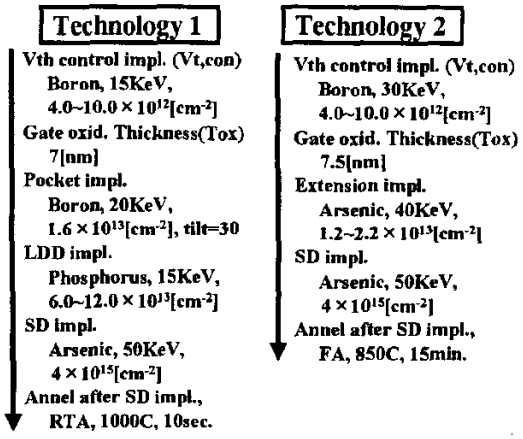

Fig.3 Process conditions (technologies 1 and 2)

distributions. The dopant pile-up at the gate edge decreases and closes to the flat as the gate length becomes short, since there is fast diffusion near the junction between S/D and channel region. The validity of the dopant profile in the bulk region is ensured by the good agreement between experiments and simulations for the back bias dependence of Vth-L_g characteristics. The dopant pile-up with the pocket becomes larger and broader than that without the pocket. The calibrated profile is comparable to the profile extracted from our inverse modeling approach [4]

The increase in number of process parameters to be optimized affects a TAT of the device design. The relation between total number of parameters and calculation time is listed in table 2. For device optimization and statistical analysis based on the design of experiments, the calculation time for 77 jobs which is more than 3 days for pair diffusion model is reduced less than 4 hours using our model. For the case of the calibration, the difference of the calculation time becomes more serious since we have to repeat this process many times. Thus, the device optimization in a short period is possible using our model.

V. CONCLUSION

We have presented an effective model for the dopant pile-up and applied to RSCE of nMOSFET. The drastic reduction of calculation time and device optimization term are possible using our model. Calibration is easy because of a few physical parameters and a clear relation between parameters and electrical characteristics. Our model is also possible to predict electric characteristics and dopant profiles for different device technologies, and our useful approach is effective for the design of advanced devices in which a quick turn around time (TAT) is required thoroughly.

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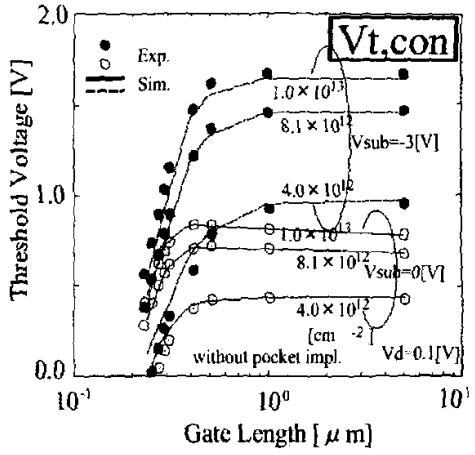
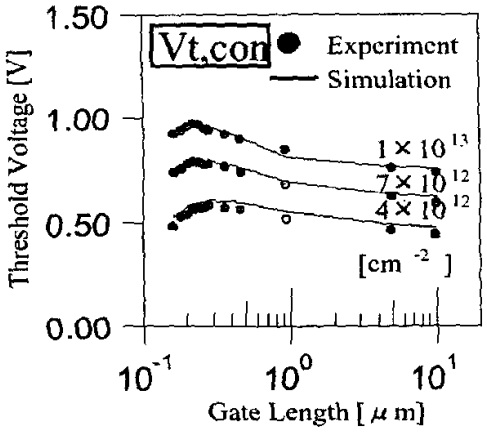
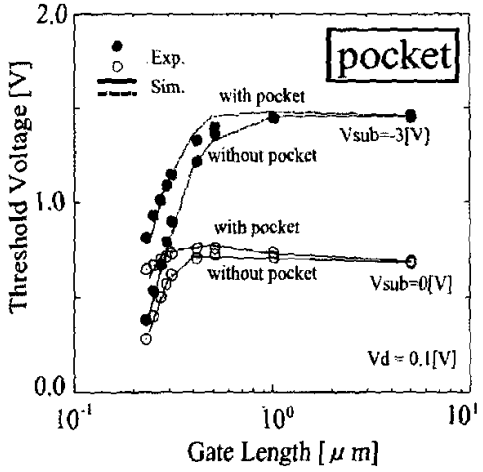
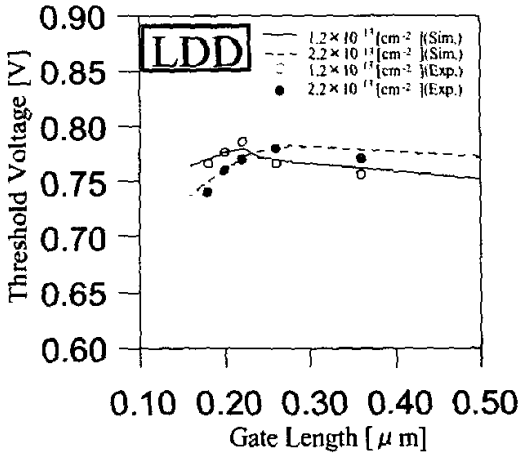
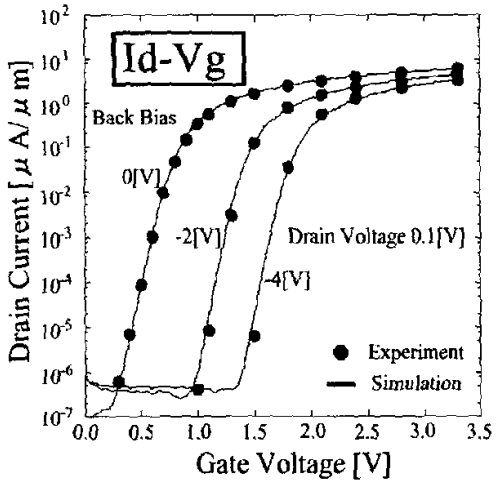










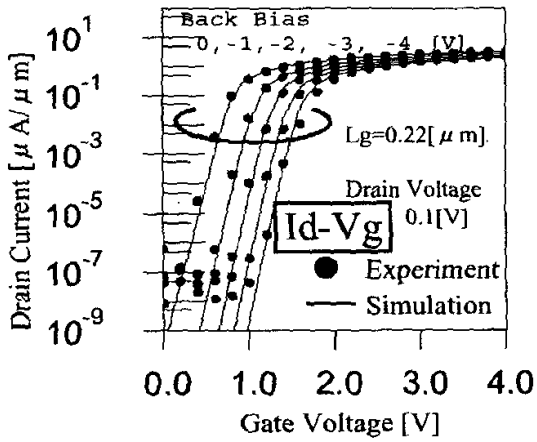
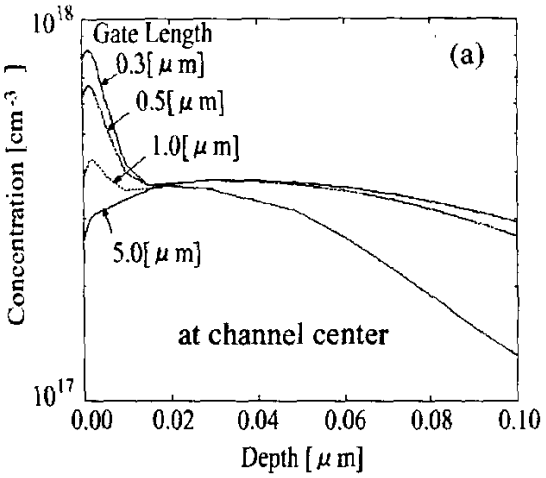


Fig.4 Electrical characteristics for various process conditions (technology 1)

Fig.5 Electrical characteristics for various process conditions (technology 2)



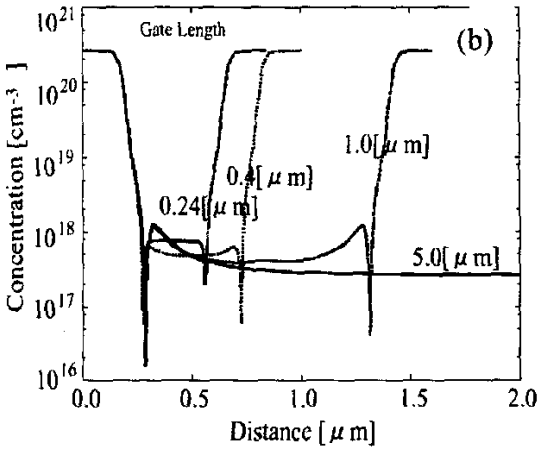


Fig6 (a)Depth and (b)lateral dopant profiles for different gate lengths (technology 1)

Table 1 Final parameter sets

Parameter	Technology1	Technology2	Unit
A	4.3×10^{-2}	5.7×10^{-3}	—
λ_1	2.00	2.00	μm
λ_{2x}	1.8×10^{-2}	1.0×10^{-3}	μm
λ_{2y}	0.15	0.50	μm

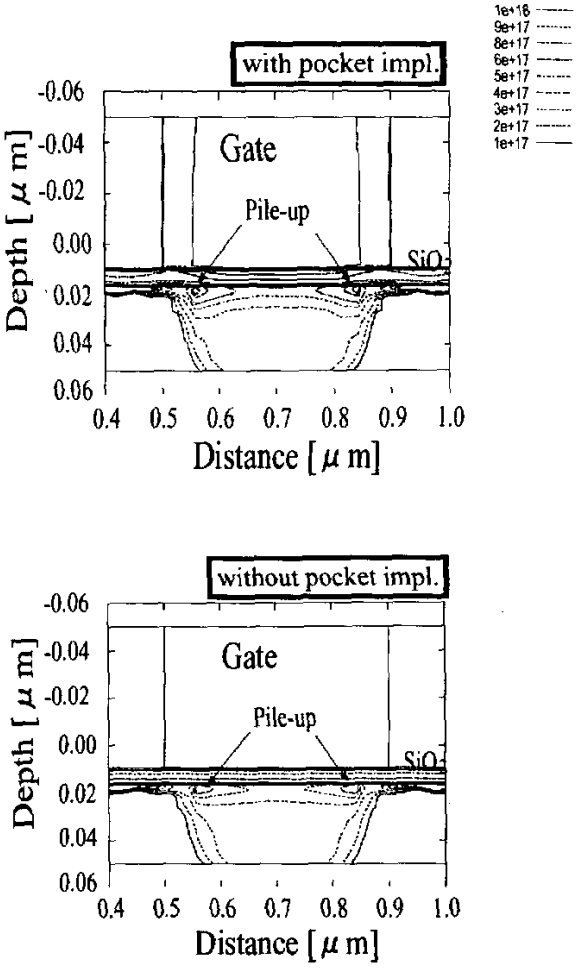


Fig.7 Comparison of 2D dopant profiles

Table 2 Comparison of calculation time (more than 1 order)

Number of Parameters	Number of Jobs	Calculation Time [hrs]	
		Present Method	Pair Diffusion
3	15	0.75 [hrs]	15.25 [hrs]
4	25	1.25	25.42
5	49	2.45	49.82
6	77	3.85	78.80

Present Method : 2 min./job for 3978 grids (DEC Alpha 667MHz)
Pair Diffusion Model : 1 hour/job,
Device Simulation : 1 min./job