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Bias-dependent drift resistance modeling for accurate DC and AC simulation of asymmetric HV-MOSFET

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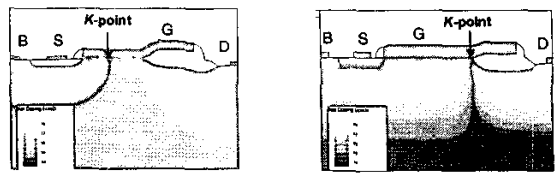
Abstract **- A detailed investigation of the drift resistance evolution with the gate and drain biases in Lateral DMOS architectures is reported. The extractions are performed using the concept of intrinsic drain voltage, V_K, applied to both simulated and measured data. Some new special test structures (MESDRIFT) have been designed and fabricated in order to investigate the DMOS bias-dependent drift resistance and experimentally confirm 2D numerical simulations. Some of the physical origins, associated with drift resistance dependence on gate and drain bias, are discussed. A simple yet efficient DMOS macro-modeling strategy is reported. It consists of combining a low-voltage BSIM model module with a bias-dependent series resistance described by a quasi-empirical mathematical expression. All LDMOS operation regimes (including quasi-saturation) are captured by the proposed expression and data measured on MESDRIFT is used to calibrate the BSIM and drift parameters. The methodology does not dependent on the drift architecture and can be applied to any similar asymmetric HV MOS devices.**

I. INTRODUCTION

High Voltage (HV) Lateral MOSFETs are extremely interesting for automotive and RF applications and require accurate analytical models and/or macro-models for advanced IC design and simulation. A key bottleneck for the modelling of LDMOS devices is the non-linear bias-dependence of their drift resistance on drain and gate voltages, $R_D(V_D, V_G)$. Generally, this dependence is complex and specific to the architecture of the extended drain region of the HV MOSFET, which is particularly engineered to sustain high voltages. Specific phenomena dictated by the drift region, like quasi-saturation, [1], (the origins of which could be related to various physical phenomena such as JFET-like control of the depletion regions or carrier velocity saturation in drift) are reflected in and thus, very difficult to be captured in an analytical compact model.

II. DEVICE ARCHITECTURES

Two Lateral HV MOSFET architectures, fabricated with a 0.7μm CMOS technology of Alcatel Microelectronics, are investigated: a double diffused n-channel (LDMOS) and a drain-extended n-channel (XDMOS) device (see Fig. 1). Both provide 100V breakdown capability. Some special test structures, called MESDRIFT (Fig. 2), were designed and fabricated to directly access the internal V_K potential and to experimentally confirm the usefulness of the intrinsic-drain voltage concept, previously proposed in [2]. The n^+ implanted contact in Fig. 2 (called in this work *K-contact*), placed in the drift region as close as possible to the p-n junction, is the only difference between typical HV DMOS devices and corresponding MESDRIFT test structures. The K-contact is designed with dimensions much smaller than the transistor width and consequently, no significant influence is expected on the overall transistor characteristics. Fig. 3 reports a comparison between transfer, I_D-V_G, and output, I_D-V_D, characteristics measured on both X-DMOS and its corresponding MESDRIFT: the very good matching of their characteristics (less than 10% difference in terms of current) appears to support the claim that fabricated MESDRIFT accurately reproduces the I-V behavior of the HV DMOS, including drift resistance bias dependence. Only a slight reduction of the breakdown voltage (<5%) is observed in case of MESDRIFT.



(a) (b)

Fig. 1. Cross section of: (a) n-channel LDMOS and (b) n-channel XDMOS architectures. Inset: K-point location

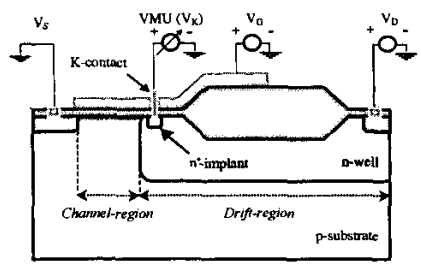
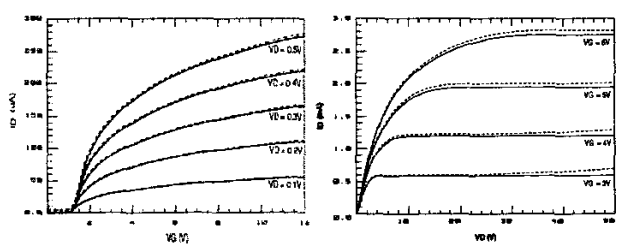


Fig. 2. Cross-section of the MESDRIFT structure with n^+ implant location and HP-4156 measurement setup used to monitor the intrinsic drain potential, V_K.



(a) (b)

Fig. 3. Experimental comparison between MESDRIFT (dashed line) and original n-channel XDMOS (solid line) in terms of: (a) I_D-V_G, and (b) I_D-V_D.

III. BIAS-DEPENDENT DRIFT RESISTANCE

In order to extract and model the DMOS drift resistance evolution with V_D and V_G, detailed 2D numerical simulations were performed with a calibrated structure. DC characteristics have been simulated and, the internal potential distribution at each (V_D, V_G)

bias point in the 2D structures has then been used to probe the intrinsic drain voltage value, V_K. The drift resistance, R_D, is extracted in a straightforward manner, based on the variable drift region voltage drop, V_D-$V_K(V_G, V_D)$, and the corresponding drain current, I_D:

$$R_D \equiv R_{drift} = [V_D - V_K(V_D, V_G)] / I_D \qquad (1)$$

With the measurement set-up based on a HP-4156 parameter analyzer, the potential of MESDRIFT K-contact (V_K) has been experimentally monitored with a high impedance voltmeter, while varying the drain and gate bias in all operation regimes of the DMOS transistor. From the monitored evolution of V_K with V_D and V_G, the bias-dependent drift resistance was calculated with eq. (1) and, the results are reported together with the numerically simulated R_D (V_D, V_G) in Fig. 4. First remark is that, at constant V_G, R_D can increase by near two orders of magnitude with V_D due to the depletion region that forms in the drift region. At low V_G, a depleted area always exists in the drift zone, below the gate oxide or the bird's beak, depending on the V_D values, which results in an increased equivalent resistance. By increasing V_G, due to the combined effects of the accumulation and carrier injection phenomena, this depleted area could disappear and, consequently, the R_D resistance decreases. A less usual behavior is observed from numerical simulated drift characteristics at low V_D values (less than 1V): R_D appears to decrease with V_D at any V_G (Fig. 4). This can be explained by the change of the conduction from surface into volume, resulting in an equivalent mobility increase, when V_D increases. When extracting R_D from the MESDRIFT devices, this phenomenon is not visible due probably to the slightly shifted location of the n^+ implant (Fig. 2). Except this particular small discrepancy, it is found that experimental $R_D(V_D, V_G)$ correctly follow the predictions of numerical simulations in *all significant operation regimes*, which confirms the validity of the V_K concept.

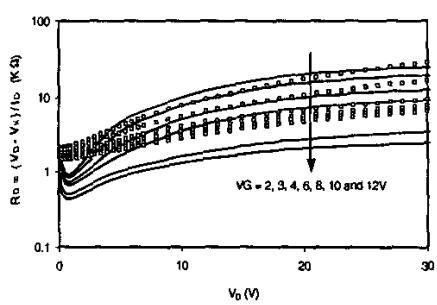


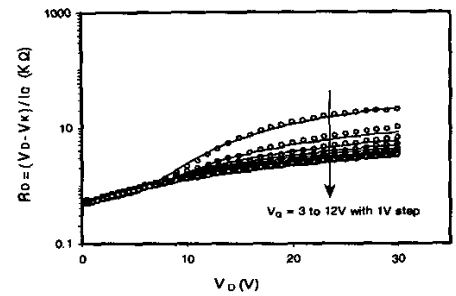
Fig. 4. $R_D(V_D, V_G)$ characteristics for XDMOS: numerical simulation (solid line) compared to measurements using MESDRIFT test structure (squares).

IV. QUASI-EMPIRICAL DRIFT MODEL

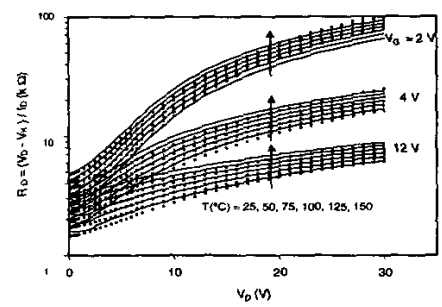
Based on the experimental and simulated reported bias-dependence of the drift resistance, we have investigated the most appropriate mathematical formulations able to properly describe $R_D(V_D, V_G)$. The following continuous mathematical, quasi-empirical expression is proposed for the drift resistance:

$$\left.\begin{aligned} R_D(V_D,V_G,T) &= (A \times B)\left(\frac{T}{T_0}\right)^{X_T} \\ A &= r_{D0} + r_{D1}/(\gamma V_G - 1) \\ B &= ln\left(e^{(\beta_1 V_G+\beta_0)V_D-(\delta_2 V_G^2+\delta_1 V_G+\delta_0)} + 1\right) \\ X_T &= (mV_D + n)^{-1} \end{aligned}\right\} \qquad (2)$$

where, r_{D0}, r_{D1}, γ, β_1, β_0, δ_2, δ_1 and δ_0 are model parameters for room temperature modeling, while m and n are parameters for the temperature dependence of R_D. Fig. 5 reveals the very good fitting of expression (2) compared to extracted drift resistances from both MESDRIFT mirroring LDMOS and XDMOS architectures. The accuracy of eq. (2) compared with MESDRIFT data obtained for XDMOS drift resistance, is better that 15% in terms of maximum error (and 4% in terms of mean error), from 25°C up to 150°C. An attractive feature of the proposed drift quasi-empiric model is its capability of acceptably tracking the R_D (V_D, V_G) characteristics of different DMOS (drift region) architectures with a unique expression (only the model parameters have to be re-tuned).



(a)



(b)

Fig. 5. R_D (V_D, V_G) of (a) n-LDMOS at room temperature and (b) n-XDMOS at various temperatures (25°C up to 150°C): experiment (symbols) compared with model of eq. (2) (solid line).

V. DC MODELING WITH V_K

In the following, we propose a modelling strategy exploiting the original features of the MESDRIFT structure. Moreover, our strategy exploits the remark that the V_K quantitative analysis in both LDMOS and XDMOS architectures confirmed that its value remains at reasonably low voltage (V_K <10V), over the entire V_D (up to 100V) and V_G (up to 12V) range of operations. It follows that the intrinsic MOSFET can be acceptably modelled using the standard low-voltage BSIM model, [2]. As a result, a simple circuit, made by the series connection of a low voltage MOS transistor (modelled with BSIM) and a bias-dependent resistor described by eq. (2) is proposed (see Fig. 6).

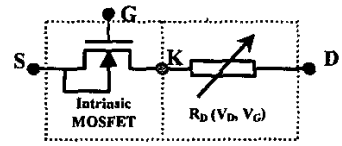


Fig. 6. Proposed circuit for the HV DMOS transistor.

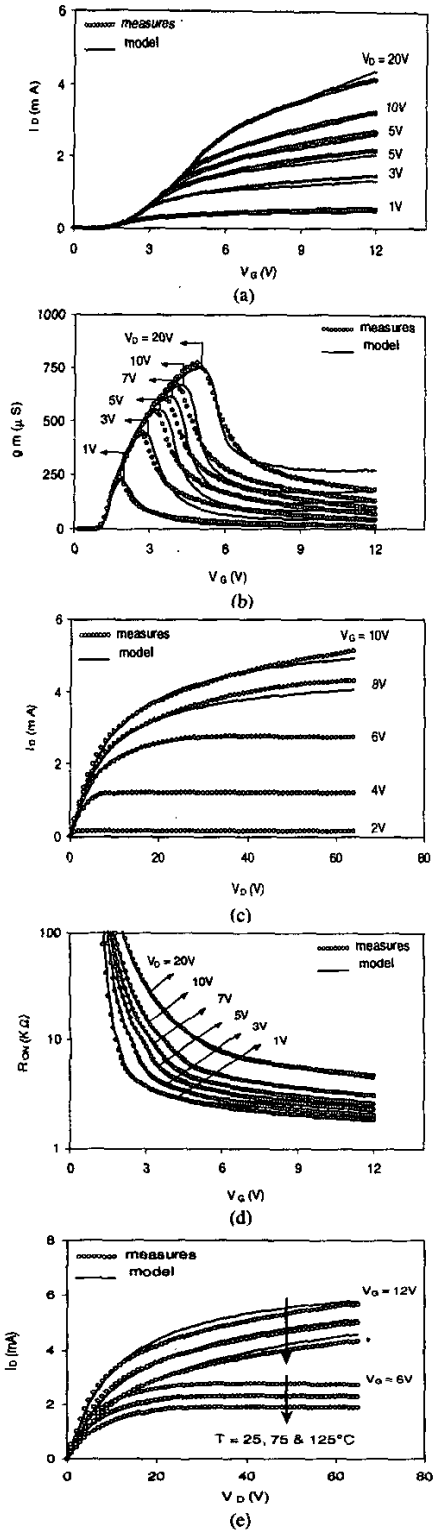


Fig. 7. Measured and modeled extrinsic characteristics (a) I_D - V_G, (b) g_m- V_G, (c) I_D - V_D and (d) R_{ON} - V_G at room temperature and (e) I_D - V_D at different temperatures, on a standard n-channel X-DMOS test device (no K-contact).

The proper modeling of the drain current is possible via a simple yet efficient modeling methodology. The first step is to monitor the V_K potential from the MESDRIFT structure, while varying the external biases, V_D and V_G over all regimes of operations. With eq (1), the R_D (V_D, V_G) characteristics are extracted, and, then, the drift expression proposed in eq.(2) is calibrated. The value of the drift resistance at low V_D (see parameter r_{D0} in eq. (2)) can be extracted with an experimental dedicated method [3]. The other parameters are extracted by an optimization method carried out on different regions on which the impact of various parameters is the most significant. The BSIM3v3 module is calibrated on the intrinsic MOS output characteristics (I_D- V_K with V_G as a parameter). The intrinsic MOS characteristics (revealed by MESDRIFT), I_D-V_G, at low V_{KS}, are reconstructed and used to estimate the threshold voltage and the low field mobility parameters.

In order to check and validate our modeling methodology, both modules of the simple circuit proposed in Fig. 6, have been implemented in SPICE. A global fitting procedure using the measured *I-V* characteristics of a standard XDMOS architecture (without K-contact) was finally performed. Fig. 7 reveals the good fitting accuracy achieved on measured data with our modeling approach: less then 15% for maximum error, including quasi-saturation region, is obtained. Moreover, the accuracy of the fitting still remains below 20% in terms of maximum error at temperature up to 125°C (see Fig. 8, e).

VI. AC MODELING WITH V_K

Another interesting finding is that V_K voltage can be used in order to properly model the HV-DMOS bias-dependent capacitances. Based on the DMOS small-signal AC circuit reported by [4], Fig. 8, and including the possibility to relate C_{GS}, C_{GD}, C_{SG} and C_{DG} to V_K, drift and channel resistances, r_d and r_{ch} respectively, we have derived the following analytical expressions:

$$C_{GS} \cong \frac{\frac{r_d}{r_{ch}} + g_{ch}.r_d}{1 + \left(\frac{r_d}{r_{ch}}\right) + g_d.r_d} \cdot C_{drift} \tag{3}$$

$$C_{GD} \cong \frac{1}{1 + \left(\frac{r_d}{r_{ch}}\right) + g_d.r_d} \cdot C_{drift} \tag{4}$$

$$C_{SG} \cong \frac{\left(\frac{r_d}{r_{ch}}\right) \cdot \left(1 + \frac{r_d}{r_{ch}} + g_{ch}.r_d\right)}{\left(1 + \frac{r_d}{r_{ch}} + g_d.r_d\right)^2} \cdot C_{drift} \tag{5}$$

$$C_{DG} \cong \frac{(1 + g_d \cdot r_d) \cdot \left(1 + \frac{r_d}{r_{ch}} + g_{ch}.r_d\right)}{\left(1 + \frac{r_d}{r_{ch}} + g_d.r_d\right)^2} \cdot C_{drift} \tag{6}$$

where C_{drift} is the oxide capacitance associated with the drift region (extension of the gate over drift), $r_d = (V_D - V_K) / I_D$ and $r_{ch} = V_K / I_D$. The transconductances of the lateral channel region (g_{ch}) and drift region (g_d) are calculated as following:

$$g_d = \left(\frac{\partial I_D}{\partial V_{GS}} + \left(\frac{1}{r_d}\right) \cdot \frac{\partial V_K}{\partial V_{GS}}\right) \cdot \left(1 - \frac{\partial V_K}{\partial V_{GS}}\right)^{-1} \tag{7}$$

$$g_{ch} = \frac{\partial I_D}{\partial V_{GS}} - \left(\frac{1}{r_{ch}}\right) \cdot \frac{\partial V_K}{\partial V_{GS}} \tag{8}$$

Typical plots of the drift and intrinsic channel transconductances, g_d and g_{ch}, respectively, are reported in Fig. 9. The combination of bias dependent g_d and g_{ch} at high V_D can

explain the typical peaks observed in the C_{SG} and C_{DG} capacitances of HV DMOS devices. It is worth noting that the proposed AC small signal model needs only the extraction of V_K (V_D, V_G) and its first derivative dV_K/V_G, in all regions of operations, which is experimentally achievable by the use of the proposed MESDRIFT structure.

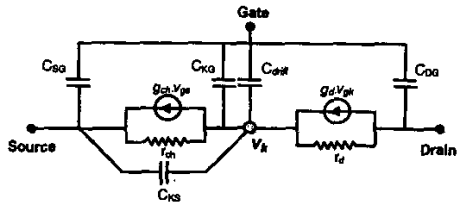


Fig. 8. DMOS small-signal equivalent circuit used for the capacitances calculations based on V_K.

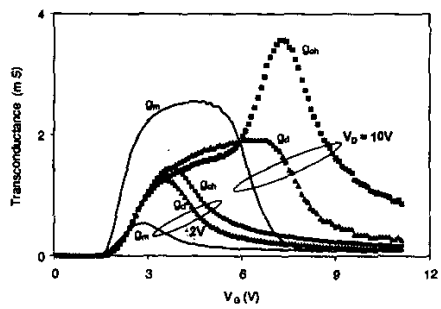


Fig. 9. Drift and intrinsic channel transconductances, g_d (tringles) and g_{ch} (squares), calculated using eqs. (7) and (8), respectively, for two different drain voltages, in case of XDMOS. Also reported in this figure: the (extrinsic) XDMOS transconductance, $g_m = dI_D/dV_G$ (solid line).

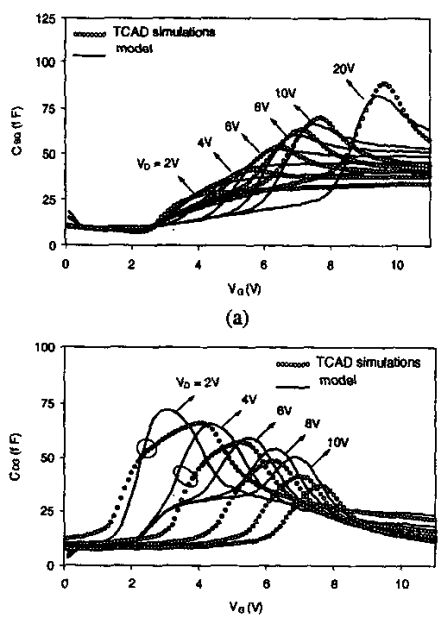


Fig. 10. (a) C_{SG}-V_G and (b) C_{DG}-V_G with V_D as a parameter: numerical simulations (circles) versus model (solid line) using eqs. (5) and (6), respectively, for n-channel LDMOS.

Systematic AC numerical simulations with the XDMOS and LDMOS 2D TCAD structures have been conducted by applying a small signal on the gate electrode (10mV, 1MHz), in all the regions of operation described by static bias combinations (V_D, V_G). At each bias point, the C_{SG} and C_{DG} capacitances have been extracted by Silvaco's ATLAS simulator, [5]. From DC numerical simulations, the values of V_K potential and its first order derivative dV_K/dV_G, at each bias point (V_D, V_G), needed for r_d, g_d, r_{ch}, g_{ch} calculations in the small-signal model, have been directly probed near the intrinsic channel end, drift side. With these values, we calculated the plots of the C_{SG}, C_{DG} capacitances presented in Figs 10 (a) and (b) and compared with values from AC numerical simulations and S-parameter extractions (after pad de-embedding). The good agreement observed between our AC model and numerical simulations reported in Fig. 10 supports the claim that, with the proposed capacitance model, it is possible to predict the peaks observed in HV-DMOS capacitances (which is the typical signature of the evolution of the drift depleted regions, onset of quasi-saturation and lateral doping profiles, [6]), as well as the capacitance evolution with V_D and V_G.

CONCLUSION

In this work, we have demonstrated the usefulness of the intrinsic drain-voltage concept for accurate DC (bias-dependent drift resistance) and AC modeling (bias-dependent capacitances) of two different HV asymmetric DMOS architectures, based on measurements carried out on a new dedicated structure and, 2-D numerical simulations.

We have proposed and validated a quasi-empirical mathematical expression for the bias-dependent DMOS drift resistance. A BSIM3v3 core has been combined in series with a bias-dependent resistance in order to model the DC characteristics of two DMOS devices (X-DMOS and L-DMOS). It should be mentioned that, despite its empirical drift formulation, the proposed V_K-modeling strategy has some clear advantages: (i) the extracted BSIM parameters have physical values (because R_D is accurately modeled), (ii) can be generalized to *any* asymmetric MOSFET with *any* bias-dependent drift series resistance architecture, (iii) very good convergence is achieved, (iv) V_K information can be used to properly identify the operation regimes of *intrinsic* MOSFET, and (v) needs relatively simple measurements for model calibration, using MESDRIFT structure.

AKNOWLEDGEMENTS

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