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# Characterization of Multi-Barrier Tunneling Diodes and Vertical Transistors using 2-D Device Simulation

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*Abstract* – **A novel memory cell which adopts a floating gate device with the writing mechanism of direct tunneling through the multiple tunnel junction(MTJ) was proposed recently. The device is known to have potential advantages of scalability, high density, high speed, long data retention time, low voltage operation, low power consumption and good endurability. Characterization and optimization of the vertical transistor with MTJ enables the construction of a novel high-density memory with high speed writing and long data retention time. This paper presents a numerical analysis of the tunnel barriers in explaining I-V characteristics of the vertical transistor. We have characterized the vertical transistor with double and triple barriers from the point of view of the central barrier. We have also performed extensive 2-D device simulation for multi-barrier tunneling diodes and vertical transistors with various device parameters. Results of the present analysis are expected to provide guidelines for designing the experiments for optimal transistor fabrications.**

## I. Introduction

Recently, the multi-barrier tunneling device demonstrated a possibility to overcome limitations in performance and density of existing memory devices [1,2]. At this early stage, there are great demands for simulation to provide fundamental understandings about device operation and development guidelines. Mizuta *et al.* applied a drift-diffusion (DD) simulation for the vertical tunneling transistor with a large channel length (L) of 350nm and showed a good agreement with measurements [3].

In this work, we have performed extensive two-dimensional (2-D) device simulations for multi-barrier tunneling diodes and vertical transistors with changing various device parameters. By comparing with measured currents for diodes with 20nm-thick interlayer silicon and various combinations of tunnel barriers, the validity of the device simulation with the DD model for multi-barrier tunneling devices is verified. The present study also provides detailed analysis for novel characteristics and design guidelines for the vertical transistor with double and triple barriers.

## II. Simulation Details

The structure of a vertical tunneling device is shown in Fig. 1. The device is composed of the vertical transistor for writing and storage of data, and a planar transistor for sensing the data in a vertical stack structure. The device is a floating gate device similar to the FLASH memory. Charges stored in the floating gate change the threshold voltage of the sensing transistor, so that the data-1 and the data-0 are distinguished to each other. The storage charges are supplied through the drain of vertical transistor and transported through a multiple tunnel junction (MTJ) controlled by a side-gate with the mechanism of direct electron tunneling instead of hot carrier injection or FN-tunneling.

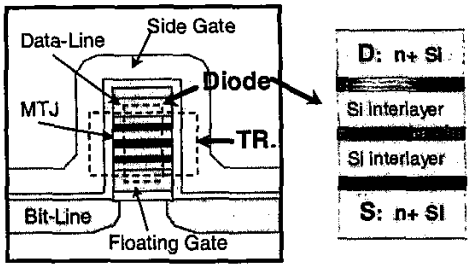


Fig. 1. The structure of the vertical tunneling device.

Simulations have been performed using a 2-D device simulator with the DD model [4]. Direct electron tunneling is computed using the Gundlach formula [5] and the self-consistent solution is obtained. Effective tunneling masses of electrons for the $Si_3N_4$(N) and $SiO_2$(O) barriers are calibrated

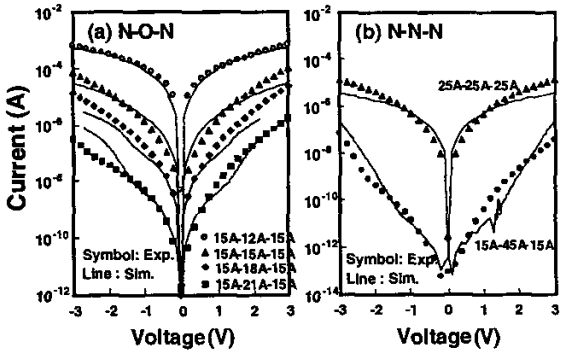


Fig. 2. Measured and simulated currents for triple-barrier tunneling diodes with (a) N-O-N and (b) N-N-N barrier combinations.

to the measured currents for single-barrier diodes. The barrier heights are specified with electron affinities, which are determined to be 2.17 and 0.97 eV for $Si_3N_4$ and $SiO_2$ barriers, respectively.

Fig. 2 shows the current density versus voltage curves for a two-terminal diode structure with three barriers. In obtaining I-V curve, the drain of the two-terminal diode is sweeped from –3V to 3V and terminal currents are calculated. Measurements and simulations are compared for multi-barrier tunneling diodes containing 20nm-thick silicon interlayer with three tunnel barriers with different thickness and layer combinations ((a) N-O-N and (b) N-N-N in Fig. 2). Agreements between measured and simulated currents are very good and this result indicates that the tunneling behaviors of the vertical tunneling devices can be described reasonably even for a very thin silicon interlayer by employing the DD simulation with electron tunneling.

## III. Vertical Transistor – Double vs. Triple Barrier

Fig. 3 shows the gate characteristics of vertical transistors with double barriers - at source and drain - and triple barriers including the central barrier. The structure with double barriers exhibits a larger ON-current compared to the triple barrier structure. Large leakage currents flow through the center of the channel at a high drain bias when the central barrier exists, which was already observed in the previous Monte Carlo simulation [6]. For transistor simulation with the thick interlayer silicon (L=350nm), we have investigated the case for the double barrier only with source/drain barrier

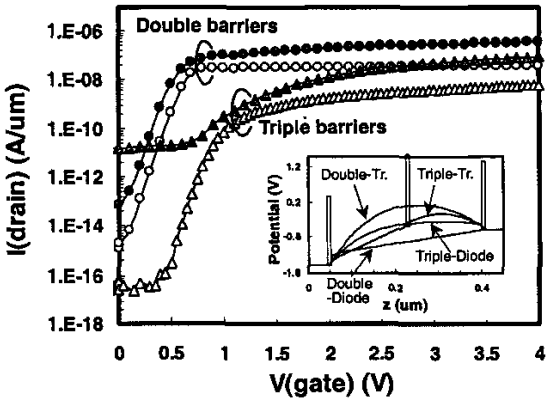


Fig. 3. Simulated Id-Vg characteristics of the vertical transistor (double barrier vs. triple barrier). The vertical channel length and lateral width are 350 nm and 200 nm, respectively. The interlayers are intrinsic silicon. All barriers are 1.5 nm thick $Si_3N_4$. The side-gate is p-doped poly and the gate oxide thickness is 7.5 nm. Empty and filled symbols denote results for the drain bias of 0.1 and 1.0 V, respectively.

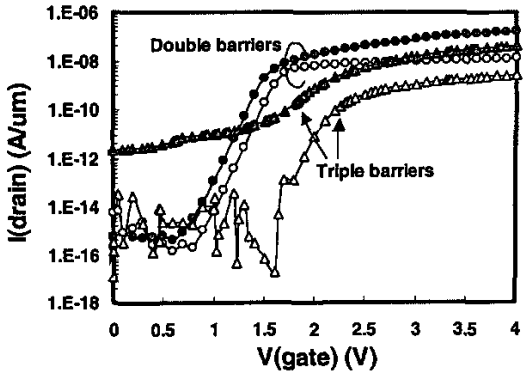


Fig. 4. Simulated Id-Vg characteristics of the vertical transistor. The vertical channel length is 100 nm and the interlayer silicon is p-type doped to 1e18 $cm^{-3}$. Others are the same with those in Fig. 3. The Si interlayer thickness is 100nm (W=200nm). Empty and filled symbols denote results for drain bias of 0.1 and 1.0V, respectively.

and for the triple barrier with the central shutter barrier. The central barrier weakens the effects of the side gate on the potential barrier in the channel, which is clearly observed by comparing potential profiles at the center of the vertical channel with those of diodes for double and triple barriers (see the inset figure in Fig. 3). As a result, the ON/OFF current ratio gets worse at a high drain bias by introducing the central barrier.

Fig. 4 shows the results for the transistor with the smaller channel length of 100nm. For such a comparatively small channel length, in which the gate controllability is significantly reduced and the center of the channel is tied to the source and drain, it may be presumed that the central barrier play a role of blocking the leakage current. However, the transistor with triple barriers is still so leaky at high drain

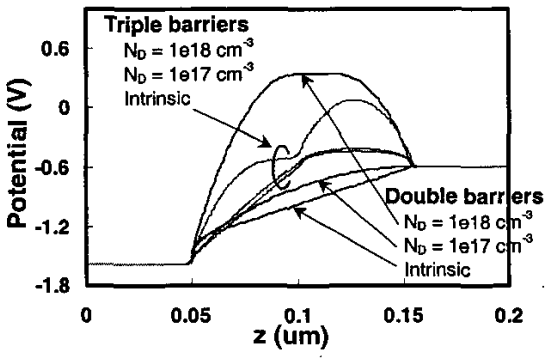


Fig. 5. Potential profiles at the center of the channel along the vertical direction of different interlayer silicon dopings (intrinsic / p-type 1e17 / p-type 1e18 $cm^{-3}$) for the diode structure. The thickness of the interlayer silicon is 100 nm.

bias and the central barrier does not play a role of reducing the OFF-current. In case of double barrier structure, the large leakage current at the high drain bias cannot be avoided with the intrinsic interlayer silicon since the electrostatic effect of the side-gate does not reach to the center of the channel and enough potential barrier is not formed. When the interlayer silicon is doped as a p-type, the leakage current decreases significantly.

Since most of leakage currents of the transistor with a small channel length are the intrinsic diode currents that flow through the center of the channel, the dependence of the diode characteristics to the interlayer silicon doping is investigated. Fig. 5 shows the potential profiles of the diode at the center of the channel along the vertical direction for different interlayer dopings. When the p-type doping level is increased to 1e18 $cm^{-3}$, a high potential barrier is developed at the center of the channel in case of double barrier structure. In case of triple barrier structure, however, the potential near the central barrier seems to be pinned and it is not so much raised as the p-type doping is increased. Fig. 6 shows the electron concentrations in the interlayer silicon at the high drain bias at the OFF- state. Electrons that tunnel from the source are blocked by the central barrier and accumulated at the source side of the central barrier. In addition, overall electron concentration of the triple barrier structure is much larger than that of double barrier. Electron blocking and accumulation by the central barrier cause the pinning of the potential and result in a large leakage current. It indicates that the large leakage current at the high drain bias is inevitable for the triple barrier structure regardless of device dimension and doping.

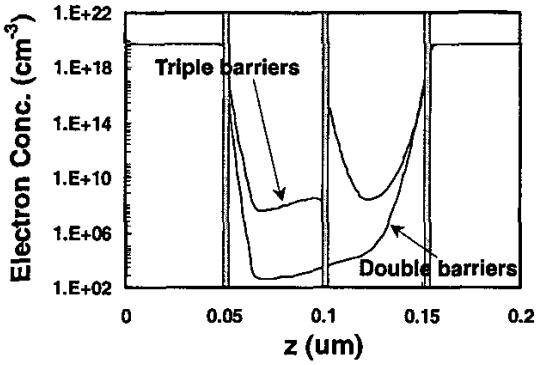


Fig. 6. Electron concentration at the center of the channel along the vertical direction for double and triple barrier when Vd=1.0 V and Vg=0.0V.

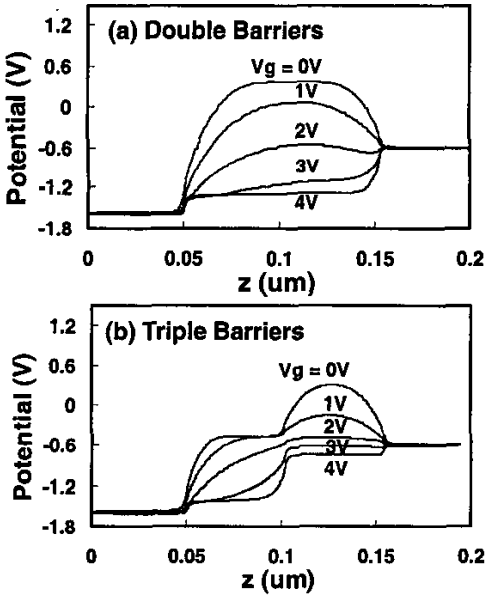


Fig. 7. Potential profile at the edge of the channel along the vertical direction for (a) double barrier and (b) triple barrier. The structure is same with that in Fig. 4.

Fig. 7 shows the potential modulation at the edge of the channel along the vertical direction according to the side-gate bias. The analysis shows that the largest contribution to the ON-current comes from the channel region near the side-gate where the potential barrier is most heavily influenced by the electrostatic effect of the applied side-gate bias. Remarkable differences are found between the double and triple barrier structures and the pinning of the potential is also found at the interface region near the side-gate oxide.

## IV. Effects of Key Device Parameters

We have performed extensive device simulation and analysis with varying the device parameters such as the vertical channel length, interlayer silicon doping, side-gate oxide thickness, and etc. Since the structure of the small vertical channel length (thin gate stack) and moderate lateral width is preferred from the process integration point of view, our extensive analysis is focused on the transistor structure having the thin interlayer silicon. Simulations are performed for various key device parameters to provide process guidelines for improving the ON/OFF current ratio and the results are shown in Fig. 8.

The dependency of the gate characteristics to the vertical channel length is shown in Fig. 8(a). It can be seen that the ON/OFF current ratio is improved by increasing the channel length, which is due to the OFF-state characteristics. The On-current, which mainly flows through the surfaces near the gate, is not reduced by increasing the channel length. The OFF-current, on the other hand, is directly influenced by the potential profile at the center of the channel and can be

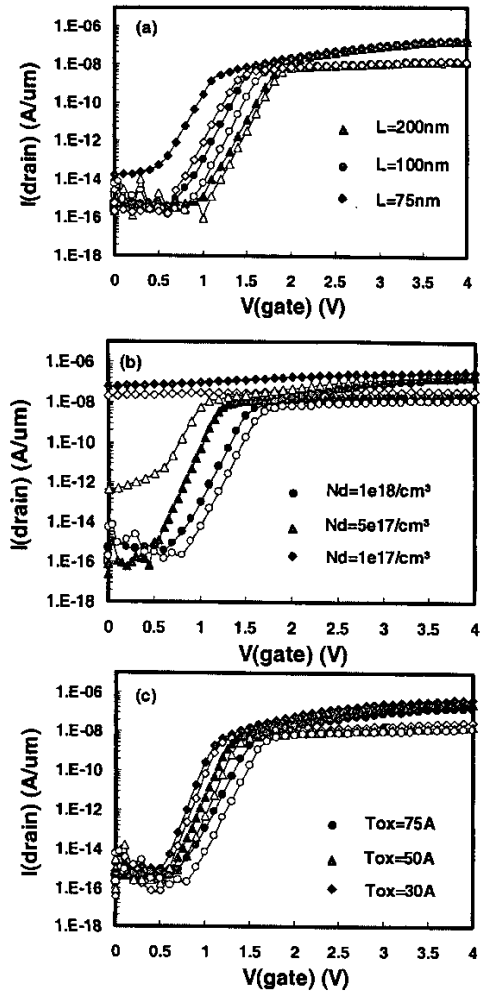


Fig. 8. Gate characteristics of the vertical transistor with double barrier at the drain bias of 0.1 and 1.0V. Simulations are performed for various device parameters such as (a) interlayer channel length (L), (b) p-type doping in the interlayer silicon (Nd), and (c) thickness of the side-gate oxide (Tox). The channel length and width are 100nm and 200nm, respectively in (b) and (c). Other device parameters are the same as those in Fig. 4. Empty and filled symbols denote results for the drain bias of 0.1 and 1.0V, respectively.

suppressed by increasing the gate stack.

Fig. 8(b) shows that the leaky tunneling current is suppressed and the ON/OFF current ratio is increased significantly for high p-type doping in the interlayer silicon. As the p-type doping increases, built-in potential barriers suppress the OFF-current through the channel. It is clear that the doping control of the interlayer silicon is the most important point to achieve novel characterristics of the multi-barrier vertical transistor. As the thickness of side-gate oxide (tox) decreases, the better subthreshold swing and reduced threshold voltage can be obtained, as shown in Fig. 8(c), which is similar to the conventional MOSFET characteristics. The OFF-state current is not small enough to ensure the non-volatility. It is not clear with the present simulation results and should be investigated further.

## IV. Conclusions

We have analyzed the tunneling behavior for multi-barrier tunneling diodes using the 2-D device simulation. For the different nitride/oxide barrier and various combinations of the barrier thickness, agreements between measurement and simulation are excellent. We have characterized the vertical transistor with the double and triple barriers from the point of the role of the central barrier. In addition, extensive 2-D device simulations for vertical transistors are performed for various device parameters. Results of the present analysis are expected to provide helpful guidelines for designing the experiments for optimal transistor fabrications.

## References

[1] K. Nakazato *et al.*, "PLED-Planar Localised Electron Devices," *Tech. Dig. IEDM.*, pp. 179-182, 1997.

[2] J. H. Yi *et al.*, "Scalable Two-Transistor Memory (STTM)," *Tech. Dig. IEDM.*, pp. 787-790, 2001.

[3] Mizuta *et al.*, "The Role of Tunnel Barriers in Phase-State Low Electron-Number Drive Transistors (PLEDTRs)," *IEEE Trans. Electron Devices*, vol. 48, pp. 1103-1108, 2001.

[4] *MEDICI User's Manual*, AVANT!, 2001.

[5] J. K. Gundlach, *Solid State Electron*, pp. 949, 1966.

[6] M. Wagner *et al.*, "A Fast Three-Dimensional MC Simulator for Tunneling Diodes," *Tech. Dig. IEDM.*, pp. 31-33, 2000.