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A Novel CDM-like Discharge Effect During Human Body Model (HBM) ESD Stress

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Abstract - **Interactions between ESD protection devices and other components of a chip can lead to complex and not easily anticipated discharge bevahior. Triggering of a protection MOSFET is equivalent to the closing of a fast switch and can cause substantial transient discharge currents. The peak value of this current depends on the chip capacitance, resistance, properties of the protection clamp, etc. Careful optimization of the protection circuit is therefore necessary to avoid current overstress and circuit failure.**

I. Introduction

Electrostatic Discharge (ESD) is generally recognized as an increasingly important issue for modern integrated circuits. Thinner gate oxides, complex chips with multiple power supplies and/or mixed-signal blocks, larger chip capacitance and faster circuit operation all contribute to increased ESD-sensitivity of advanced semiconductor products [1]. Detailed understanding of complex circuit-device interactions is essential for the design of effective ESD protection. This paper presents the analysis of a previously unreported ESD phenomenon—a CDM-like (Charged Device Model) discharge between a grounded-gate ESD protection MOSFET and the chip capacitance. The effect has serious implications for the ESD failure threshold and must be considered in the design of robust semiconductor products. An important consequence of the effect is that a circuit-level technique commonly used to reduce the Vdd and Vss power noise coupling—the addition of a decoupling capacitor—can result in strong current spikes and thus degrade ESD performance.

II. Industrial ESD Analysis

Although it has been long expected that simulation can and should serve a big role in addressing ESD issues, industrial applications have been rare. The problem has been approached from two directions: circuit simulation with added empirical high-current device models and device simulation with added mixed-mode simulation [2]. The circuit simulation approach has suffered from its non-physical nature and poor convergence. The device simulation approach has been limited to few research-type aplications because of ease-of-use problems, meshing issues and excessive simulation run times.

This paper discusses an industrial application of a novel ESD simulation tool [3], which combines physical acuracy of mixed-mode circuit-device simulation with the usability of an integrated circuit designer package. The tool provides capabilities for in-depth studies of device-level effects [4],[5] as well as analyses of larger circuits characterized by complex interactions within I/O buffer circuits embedded in their chip environments and Charged Device Model (CDM) problems [6].

Numerical analysis of industrial ESD problems poses a number of specific challenges. ESD events push circuits into high voltage and high current operation regimes posing challenges for convegence, their high speed makes the incorporation of RLC parasitics important, and the distributed nature of many discharge events necessitates the inclusion of a substantial number of active and passive elements. Ease-of-use is a critical consideration for the acceptance ESD tools, since ESD problems are typically addressed by design engineers and not a dedicated research group.

Device synthesis and automatic mesh generation are used in conjunction with inverse modeling to generate devices which assure accuracy and reasonable simulation times. Inverse modeling provides a high level of accuracyat a fraction of the engineering effort required for calibrating a conventional coupled process-device simulation flow. As an example Fig. 4 shows simulated and TLP-measured snapback curves for one of our device technologies. For the purpose of ESD simulation, it is most important to obtain accurate triggering voltage Vt1 and on-resistance values of the protection devices. Excellent agreement is evident on both linear and log scales. Calibrated finite-element level devices are stored in a library to be used by ESD circuit designers.

The ESD-relevant circuit is specified through the built-in schematic capture tool, finite-element device models are imported from the device library. The total circuit size is only limited by the available memory and CPU time. Circuits can include both finite-element level devices and BSIM3v3 level analytic devices. This allows an inclusion of larger portions of the chip circuitry in the simulation along with ESD protection devices involved in high-voltage high-current ESD discharge events As an example, Fig. 3 shows an ESD protection circuit with a finite-element level ESD clamp M10 and a BSIM3-level inverter M11, M12.

III. Transient CDM-like Discharge Effect

For our study of the nonlinear resonance effect we use a calibrated 0.24μm ESD grounded-gate MOSFET clamp connected to a 200pF chip capacitance with intrinsic 5Ω resistances of the VDD and VSS buses as shown in Fig. 4. A test circuit was set up including a Human Body Model discharge circuit with a 100pF capacitor C0, 7.5μH inductor L0 and a 1.5kΩ resistor R3. As we will see below, the inclusion of an equivalent chip resistance in the model is essential.

Fig. 5 shows the voltage waveforms on the discharging HBM capacitor and Fig. 6 the clamp/pad voltage (log time scale) for a total of four cases: two different values of chip resistance 0.5,5Ω with and without a 100pF decoupling capacitance C2. The MOSFET triggers in all cases at about 9V, then enters snapback and the clamp/pad voltages drops to the holding voltage of 4V. Clamp currents in Fig. 7 show that large spikes occur in the low chip resistance and decoupling capacitance cases. Immediately following triggering, pre-charged capacitors (chip capacitor C1 and decoupling capacitor C2)

discharge into the now highly conductive MOSFET clamp. The magnitude of this discharge current depends on the chip resistance and the on-resistance of the clamp. The effect is analogous to a Charged Device Model discharge, with the energy stored in the chip and decoupling capacitors rapidly discharged into the clamp.

Very large peak currents can be reached if the chip resistance is small or a decoupling capacitor is used. In the decoupling capacitor case "5+C2" the peak current is about 9A (Fig. 7), 7 times higher than the peak HBM discharge current. These high currents can lead to unexpected failure in metal lines or the clamp MOSFET.

Reducing the chip resistance from 5 to 0.5Ω does not significantly increase the clamp peak current beyond the already high value of 9A. Not surpsisingly however, chip current in Fig. 8 shows strong spikes for low chip resistance values. High discharge current peaks can lead to dangerous current overstress of metal lines on the chip.

IV. Current-Voltage Traces for the MOSFET

A look at the transient current-voltage dependence of the MOSFET clamp provides an interesting perspective on the high discharge current peaks described in the previous section. As seen in Fig. 9, Fig. 10, the pre-charged chip and decoupling capacitors force the clamp voltage to remain high immediately after triggering. For small chip resistance values or a large decoupling capacitor, the transition from off-state to on-state is almost vertical resulting in very large currents corresponding to the small MOSFET on-resistance after triggering. An upper limit for the current peak can be obtained as (Fig. 11):

$$I_{max} = \frac{Vtl}{R_{On}} \qquad \text{(EQ 1)}$$

This transient discharge effect leads to a loop-shaped trace in the current-voltage characteristic as shown schematically in Fig. 11. It is evident that an accurate simulation of the ESD discharge cannot be based on the DC current-voltage characteristic alone. A physical mixed-mode device-circuit simulation is essential.

V. Conclusions

We described a novel CDM-like discharge event which can occur during HBM stress. The discharge event can result in high transient currents and can lead to permanent failure in the core chip or ESD protection devices. This high discharge current is the result of an interaction between the ESD protection clamp and its chip environment and therefore makes the ESD performance of a protection circuit dependent on the product it is used in. The significance of the effect lies also in that a commonly used circuit technique of introducing additional decoupling capacitors can harm ESD performance.

VI. References

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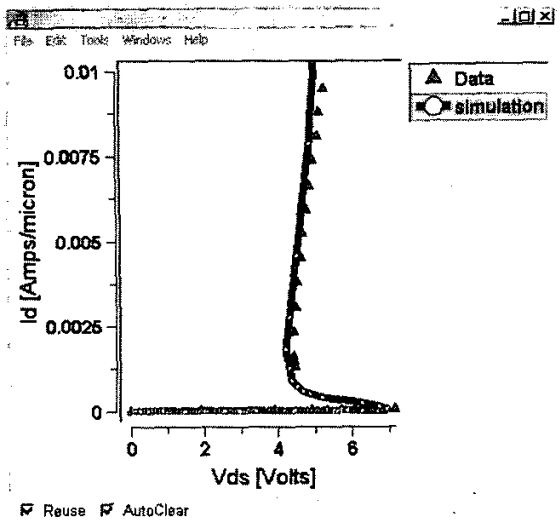

Fig. 1 Calibrated snapback simulation results and Transmission Line Pulse (TLP)-measured data for a 0.18μm technology N-MOSFET.

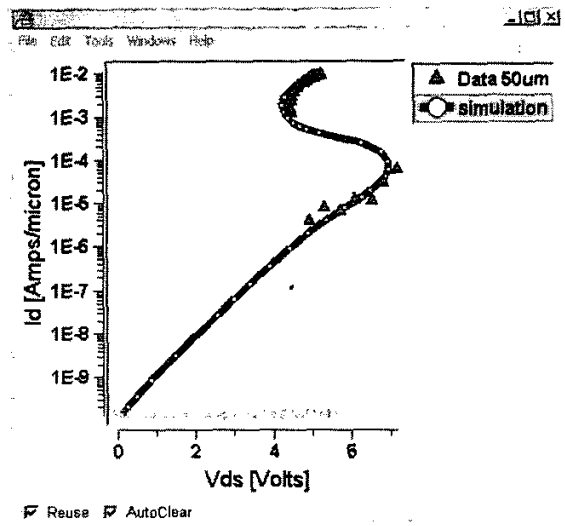

Fig. 2 Same as Fig. 1 but on a logarithmic scale.

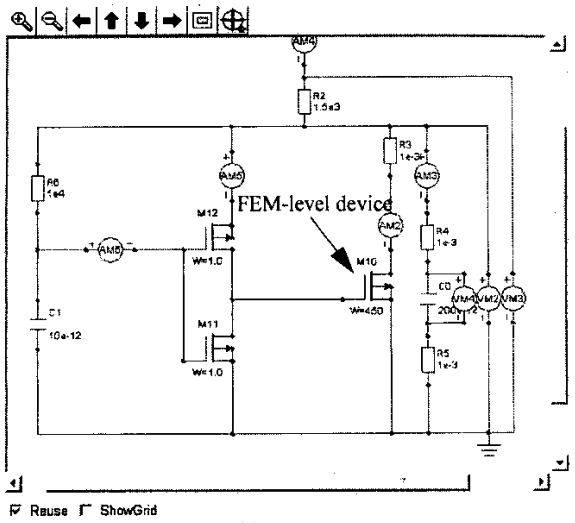

Fig. 3 Example ESD simulation circuit with a combination of one finite-element level device (M10, circled) and two analytic BSIM3-level devices M11 (NMOS) and M12 (PMOS).

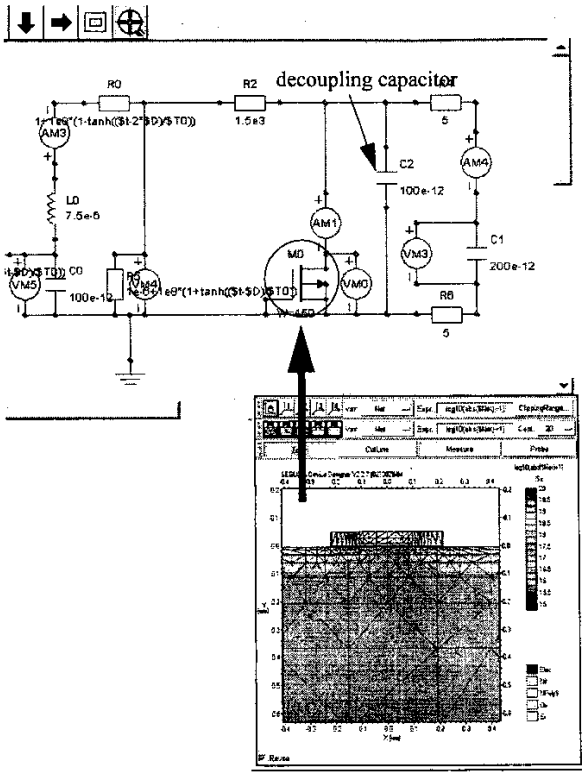

Fig. 4 ESD simulation setup with the HBM discharge circuit on the left (C0, L0, R2), protection clamp M0 (L=0.24μm, W=450μm), chip capacitance C1 and a decoupling capacitor C2. Device structure used for M0 is shown in the insert. Resistors R0, R3, R5 are time-dependent switches.

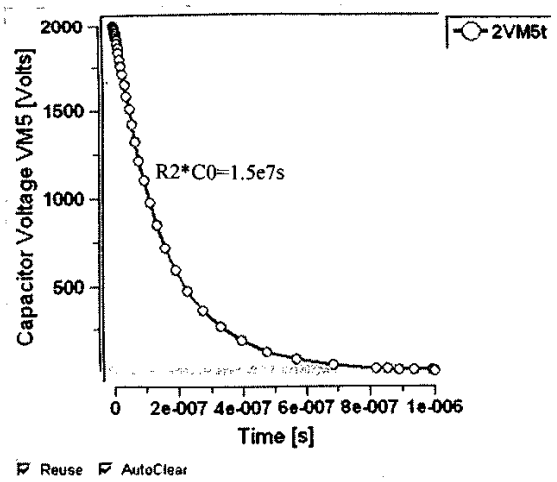

Fig. 5 HBM capacitor C0 voltage VM5 (linear time scale).

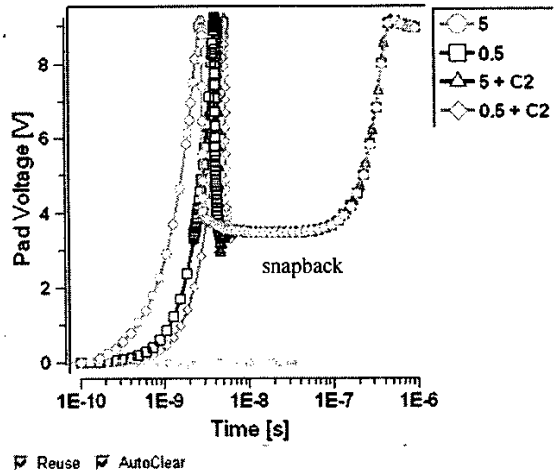

Fig. 6 Pad voltage VM0 (log time scale) for the cases: cases 5,0.5 — R4=R6=5,0.5Ω, no decoupling capacitor C2 cases 5+C2,0.5+C2 — R4=R6=5,0.5Ω and C2=100pF.

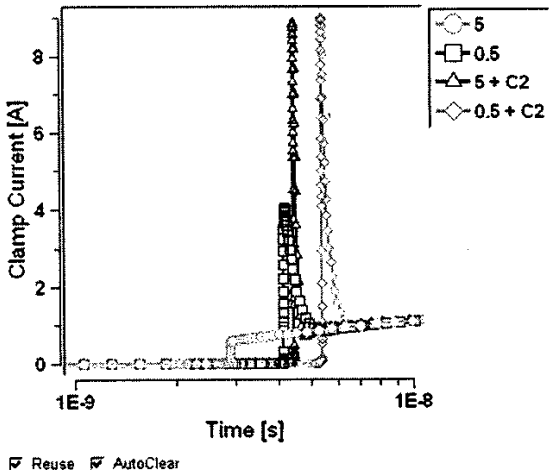

Fig. 7 MOSFET clamp current AM1 for the same cases as in Fig. 6.

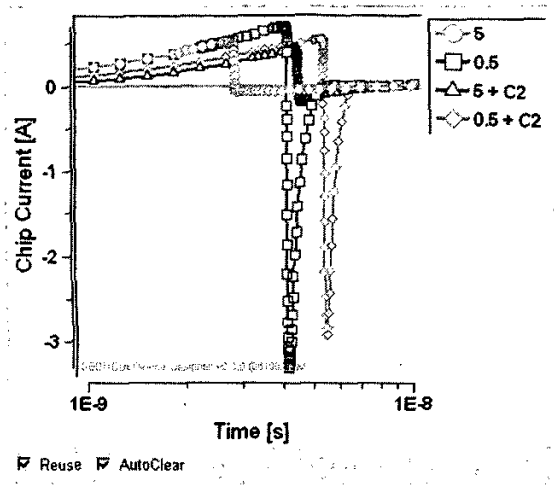

Fig. 8 Chip current AM4 for the same cases as in Fig. 6.

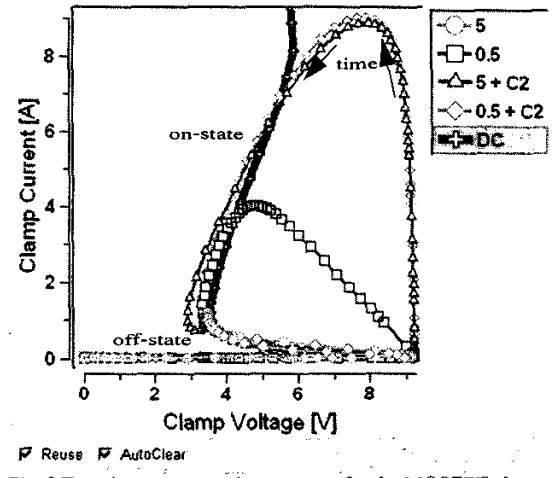

Fig. 9 Transient current-voltage curves for the MOSFET clamp for all cases as in Fig. 6 as well as DC — steady-state current-voltage characteristic.

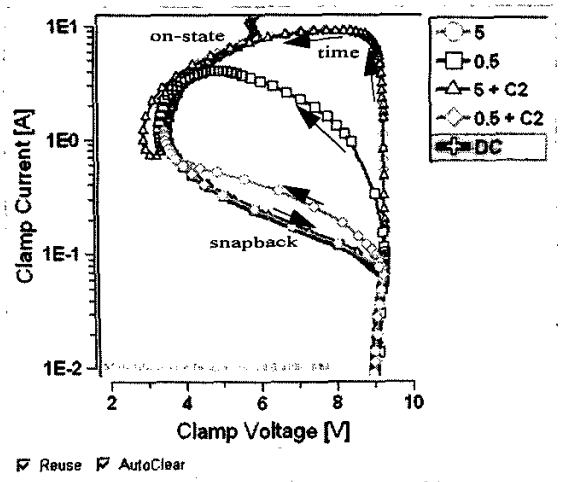

Fig. 10 Transient current-voltage curves for the MOSFET clamp on a log scale for the current axis. Cases are as in Fig. 9. Arrows indicate direction of time evolution.

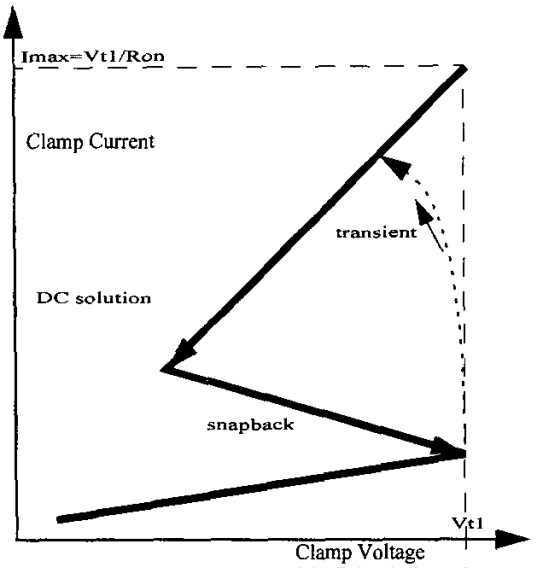

Fig. 11 Schematic representation of the DC (black) and transient responses (red, dashed) of the NMOSFET. Transient charge storage causes a loop-shaped current-voltage trace with a vertical transition from the off-state branch to the on-state branch. The transition section of the curve is not part of the DC trace, which means that a DC solution does not exist there. A finite-element level simulation is essential to capture this phenomenon, analytic MOSFET models using fitted snapback characteristics are not an adequate substitute.