Transistor Width Dependence of LER Degradation to CMOS Device Characteristics

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Abstract - **When transistor gate length is scaled down, the impact of transistor poly gate line edge roughness (LER) on device characteristics becomes significant [1]. In this work, we study the dependence on transistor width of the low spatial frequency LER induced CMOS device Ion/Ioff degradations, based on TCAD simulation results and silicon data. Methodology to account for LER effects in device optimization is also discussed. We found that when the transistor width becomes comparable to the LER spatial period, the resulting transistor Ion/Ioff degradation presents a very different signature from that of wide transistor cases. We found that for narrow width transistors, the scatter clouds on the Ion/Ioff plot stretch out along the Ion/Ioff curve direction and compress vertically toward the ideal Ion/Ioff curve resulting in transistor parametric yield loss.**

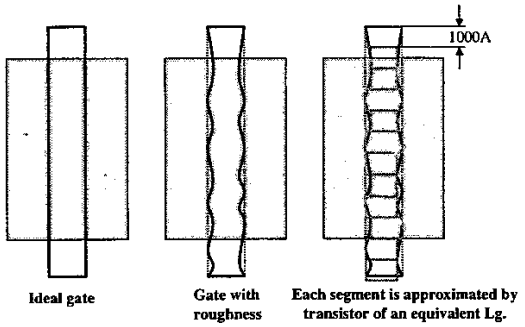
I. INTRODUCTION

CMOS transistor gate length has been aggressively scaled down in order to improve circuit performance. The impact of transistor poly gate line edge roughness (LER) on device performance becomes increasingly important [1]. Efforts to model LER effect and search for process improvements to reduce LER have been reported [2][3][4]. However, methodology to account for LER in transistor data analysis during technology development has not been discussed. At the early stages of technology development, gate patterning processes are often not mature and LER variation is typically large and unstable. Different amount of LER effect exists inevitably between different process splits. In order to identify processes which provide intrinsic performance improvement, it is important to be able to separate out LER effect from the other factors. To isolate effect from LER, one would need to find characteristics of LER which present different dependence on device parameters. In this work, we explore this subject. First, we study the dependence on transistor width of the low spatial frequency LER induced CMOS device Ion/Ioff degradations, based on TCAD simulation results and silicon data. Methodology to account for LER effects in device optimization is then discussed.

In the ideal case, without taking into account of LER effects, transistors of the same gate length L will fall onto an identical point on the Ion/Ioff plot. However, when LER effects are included, transistors with the same L, but randomly different edge shapes fall on different points on the plot, due to the different L dependence of Ids and Ioff, which results in a scatter data cloud. This scatter cloud not only spreads out but also shifts its average center relative to the ideal Ion/Ioff curve to the higher Ioff side, as discussed in several previous papers [1][3]. Earlier simulation work mostly concentrated on transistor widths much larger than LER spatial period. In this work, we look into cases where the transistor width becomes comparable to the LER spatial period. We found that the resulting transistor Ion/Ioff degradation presents a very different signature from that of wide transistor cases. We found that for narrow width transistors, the scatter clouds on the Ion/Ioff plot stretch out along the Ion/Ioff curve direction and compress vertically toward the ideal Ion/Ioff curve. Although, the average Ion/Ioff degradation appears to become smaller, the transistor parametric yield is greatly impacted, due to increased Ids and Ioff variations.

II. SIMULATIONS AND EXPERIMENTS

The simulations have been carried out using a multiple 2D device approximation similar to the method outlined in reference [3]. The width of the transistor is divided into multiple segments of 2D devices with width equals to LER characteristic spatial period, as shown in Figure 1. First, Ids and Ioff for each 2D segment are determined, then, the Ids and Ioff for each piece are summed together to give the Ion/Ioff for the whole device.



$$Ion = \sum Ids_i \quad Ioff = \sum Ioff_i$$

Figure 1 Schematic of LER simulations

In order to be able to perform large number of simulations efficiently for any randomly generated gate edge shapes, transistors with a range of gate lengths are pre-simulated, and the IV curve for any randomly generated gate length is calculated by piecewise quadratic interpolation.

Devices with gate lengths ranging from 45nm to 100nm and gate widths of 10μm, 2μm and 0.2μm have been simulated. Figure 1 shows a schematic illustration of the LER simulation approach. Figure 2 shows Ion/Ioff plots of random cases with LER of σ=4nm and gate width, W=10μm. The ideal Ion/Ioff curve for the devices without LER effects has been plotted in solid line as a reference.

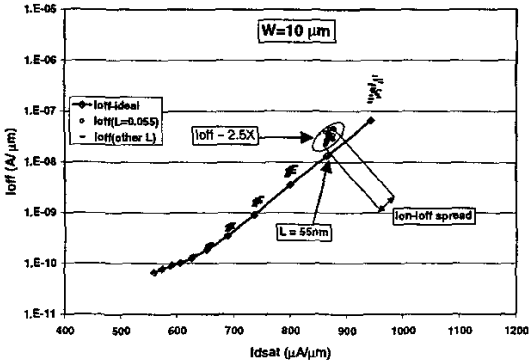


Figure 2 NMOS Ion/Ioff with LER (σ=4nm). W=10μm.

The LER characteristic spatial period used in the simulation is 100nm which represents the slow varying component of the LER. CD-AFM and SEM measurements of poly gate show that there is significant amount of slow varying component of LER at spatial period around 100nm.

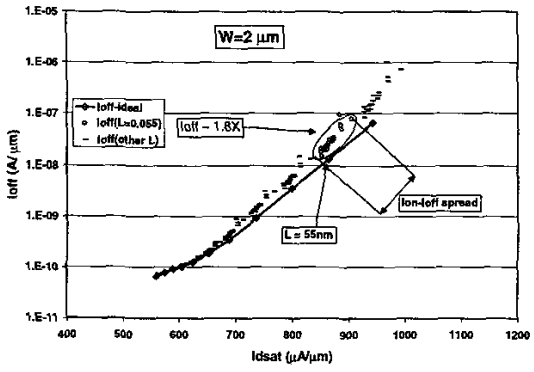


Figure 3 NMOS Ion/Ioff with LER (σ =4nm). W=2μm.

The simulation results for narrower transistors with widths equal to 2μm and 0.2μm are shown in Figures 3 and 4, respectively. The resulting data scatter clouds due to LER for transistors with different L's are plotted, where the data cloud from L=55nm transistor is circled out for examination.

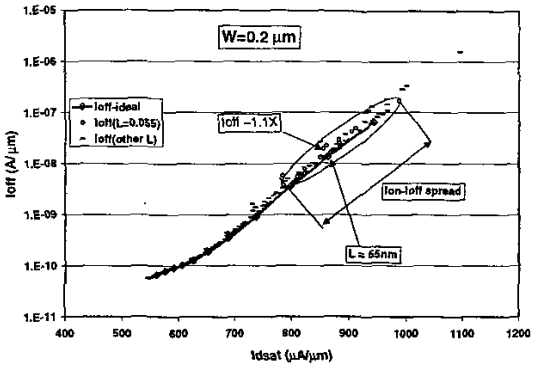


Figure 4 NMOS Ion/Ioff with LER (σ =4nm). W=0.2μm.

Comparing Ion/Ioff clouds of different transistor widths, we can observe the gradual change of the cloud shape and movement of the average distance of the cloud centroid relative to the ideal curve. As transistor width gets narrower, the spread of the data cloud along the Ion/Ioff direction increases, while the spread of the data cloud perpendicular to the Ion/Ioff direction decreases. At the same time, the average distance from the cloud centroid to the ideal curve also becomes smaller. This can be explained by examining the extreme limiting case, when the transistor width is smaller than the LER spatial period, the LER approximately translates into transistor length variations. The random samples become transistors with different gate lengths – and the scatter clouds collapse on to the ideal Ion/Ioff curve, while the spread along the Ion/Ioff curve increases.

On the first look, one would conclude that the narrow width devices seem to suffer less from LER degradation, however, when the parametric yield is considered, one needs to reduce the percentage of devices falling out of Ioff specs by targeting lower Ioff for the nominal gate length, as a result, device performance will be degraded.

III. RESULTS AND DISCUSSIONS

Based on the simulation results outlined above, LER degradation has a characteristic dependence on the transistor width. Specifically, the LER caused Ion/Ioff curve shift (average centroid degrade to the higher Ioff side) reduces when transistor width becomes smaller.

The reduced sensitivity of the narrow width device Ion/Ioff to LER could be potentially very useful in process split analysis as will be discussed in the following.

During the course of technology development, silicon results generated from various process splits are analyzed to determine the benefits of these process changes. Typically, Ion/Ioff curves are compared between different process splits. However, oftentimes, each split might have been influenced differently from LER. For instance, different split often has different Lgmin (gate length at Ioff specs), therefore, is affected differently from LER even if the LER sigma is the same. Since in modern CMOS processes, device performance improvement has to be realized through optimization of various factors, the contribution from each of the factors is often very small (many only <5% Ion/Ioff impact). In order to be able to catch such small differences, it is crucial to try to reduce the influence of LER and to distinguish the differences between the results caused by the intended process changes. Figure 5 shows an example of silicon split results.

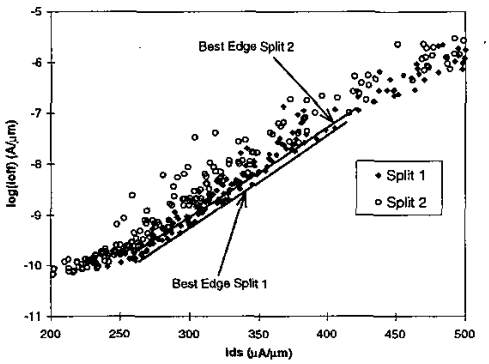


Figure 5 PMOS Ion/Ioff plots of 2 process splits results comparison between wide devices.

The measured LER sigma for this process is around 3.5nm. By examining the Ion/Ioff plots, it can be seen that split number 2 has smaller Lgmin than that of split number 1, and the average Ion/Ioff curve is also degraded. At different Lgmin, amount of LER degradations are different, where the degradation is greater when Lgmin is smaller. We found that the difference in LER degradation to Ion/Ioff is sizable enough to skew conventional interpretation of the results.

As discussed earlier, the difference in LER degradation of the Ion/Ioff curve position can be minimized if we examine the narrow width devices. Plotted in figure 6 is comparison of the narrow width devices from the same two process splits. It can be seen that the differences between the splits are now very different from that of the wide devices.

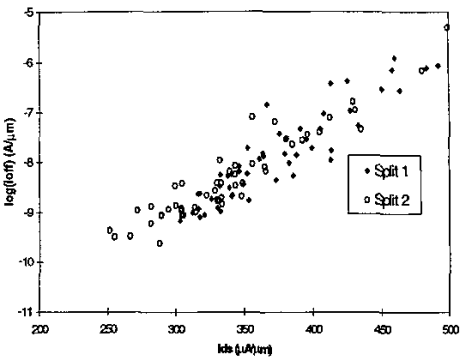


Figure 6 PMOS Ion/Ioff plots of the narrow width devices.

It is also possible to examine the best edge of the Ion/Ioff scatter cloud of each split, shown in solid lines in figure 4. Since the best edge represents the devices which happen to have smallest LER variation across the width of that specific device, one would argue that when the sample size is big, the best edge will has the smallest impact from LER. Therefore, we expect the best edge comparison could be a more accurate evaluation of the intrinsic value of the different process splits than by simply comparing the average results.

IV. CONCLUSION

In summary, we have shown that the impact of the slow varying component of the LER on the transistor Ion/Ioff characteristics is a function of the transistor width. We have found that when transistor width becomes comparable to the LER characteristic spatial period, the Ion/Ioff scatter cloud spread more along the Ion/Ioff curve and the average moves closer to the ideal curve. We further discussed a methodology to de-convolute the LER effects and process effects by examining both the best edge of wide devices' Ion/Ioff and the narrow width devices' Ion/Ioff curves.

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