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# A Comprehensive Simulation Study of Strained-Si/SiGe nMODFET Scaling for RF Applications

Qiqing Christine Ouyang, Steven J. Koester, Jack O. Chu, Alfred Grill, Seshadri Subbanna* and Dean A. Herman Jr.**
IBM T. J. Watson Research Center, Route 134, Yorktown Heights, NY 10598
*Now at IBM Sever Group, 2455 South Road, Poughkeepsie, NY 12601
**IBM Microelectronics, 2070 Route 52, Hopewell Junction, NY 12533
couyang@us.ibm.com

***Abstract*** — 2-dimensional (2-D) device simulations have been performed to study the scaling of strained-Si/SiGe nMODFETs. Device fabrication has been conducted to verify the simulation results. It is found that lateral scaling alone cannot improve the device performance. In order to achieve high speed ($f_T$ > 300 GHz), acceptable voltage gain ($G_V$ > 10) and good turnoff characteristics ($I_{on}/I_{off}$ > $10^3$) for RF applications, vertical scaling of the layer structure and source/drain junctions is also required. Preliminary experimental results support the scaling theory.

## I. Introduction

Substantial mobility improvement in modulation doped, tensile-strained silicon quantum wells has inspired recent work on Si/SiGe n-channel modulation-doped field-effect transistors (MODFETs) [1]-[4]. Compared to SiGe BJTs and RF silicon CMOS, SiGe MODFETs have potential advantages of low power, lower noise and high maximum oscillation frequency ($f_{max}$). Therefore, SiGe MODFETs are promising for future RF communication applications. In addition, their potential compatibility with standard silicon CMOS technology offers possible system-on-a-chip (SOC) applications. MODFETs with long channel lengths ($L_G$ = 0.2~0.5 μm) have demonstrated encouraging results [1]-[4]. In order to achieve higher speeds, proper device scaling is necessary. In contrast, the scaling of Si/SiGe MODFETs is fundamentally different from that of III-V MODFETs, because of the relatively lower carrier mobility and the lack of a high band gap barrier material in Si-based heterostructures. Furthermore, some of the conventional scaling techniques used in silicon CMOS technology cannot be used for Si/SiGe MODFETs due to process compromises needed to maintain the high mobility in undoped, strained layers. Certain device scaling strategies have been discussed for Si/SiGe-based FETs with *fixed* vertical structures [5], but the lateral scaling for $L_G$ < 0.1 μm has not been explored. In this paper, we report the most comprehensive study to date on the lateral scaling as well as the vertical scaling of Si/SiGe nMODFETs. 2-D device simulations have been performed in order to study various scaling effects independently, and device fabrication has been conducted to verify the simulation results.

## II. Device Structure and Simulations

The nMODFET device has a well-known structure as shown in Fig. 1. An undoped, tensile strained-Si quantum well channel (9 nm in our case) is on top of a relaxed SiGe virtual substrate. A doped SiGe layer serves as a supply layer, which can be formed above and/or below the channel with an undoped SiGe spacer layer in between (top and/or bottom doping). The depth of the quantum well is $d_{QW}$. For the particular devices with $d_{QW}$ = 25.5 nm, the doping profile taken from *previously* fabricated devices with only the top doping was used for the supply layer in the simulations, where as for the devices with $d_{QW}$ = 3 nm, a uniform, bottom-doping profile was used. The devices with zero gate-height have been simulated using the drift-diffusion model in MEDICI [6]. The relevant parameters for carrier transport have been calibrated against *previous* experimental results [3]. Fig. 2 shows the comparison of the simulated and measured $I_D$-$V_{GS}$ characteristics for a set of representative devices. Good agreement has been achieved over a wide range of device geometries, except for the current at the large negative gate biases due to the lack of a proper model for the carrier tunneling though the Schottky gate in MEDICI.

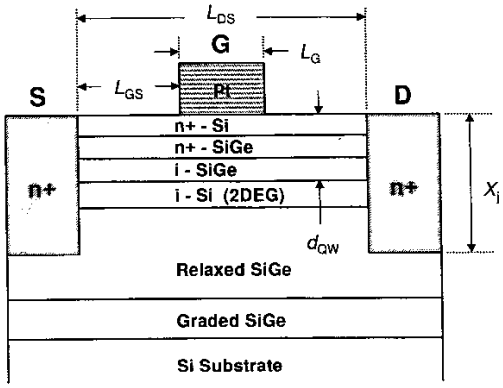


Fig. 1. Schematic of a Si/SiGe nMODFET.

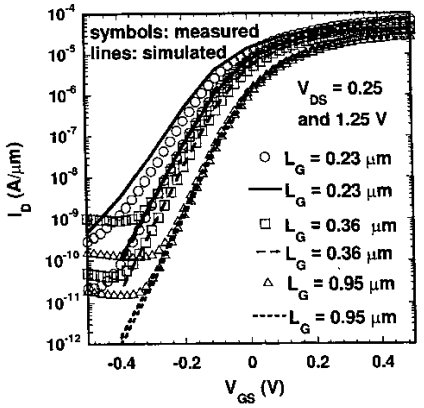


Fig. 2. Comparison of simulated and measured $I_D$-$V_{GS}$ for three representative devices with fixed layer structure ($d_{QW}$ = 25.5 nm) but different lateral geometries.

### III. Results and Discussions

Fig. 3 shows the simulated $I_D$-$V_{GS}$ characteristics for two devices with a deep channel ($d_{QW}$ = 25.5 nm). As the source-drain separation ($L_{DS}$) and gate length ($L_G$) are scaled, it becomes harder to turn off the device. Higher off-state leakage and larger output conductance ($g_d$) result in larger standby power, lower DC voltage gain ($G = g_{m\_max}/g_d$; $g_{m\_max}$: peak extrinsic trans-conductance; $g_d$: output conductance) and lower $f_{max}$. In order to improve gate control, $d_{QW}$ must be scaled, bringing the channel closer to the surface. In addition, the source/drain junction depth ($X_j$) has to be reduced in order to suppress bulk punchthrough and drain-induced barrier lowering (DIBL).

The simulations show that $L_G$ dependence of the device performance for fixed $L_{DS}$ and gate-to-source spacing ($L_{GS}$) is sensitive to $d_{QW}$. As shown in Fig. 4, for the devices with $d_{QW}$ = 25.5 nm, the $g_{m\_max}$ and peak $f_T$ are predicted to reach maximum values of 280 mS/mm and 76 GHz at $L_G$ = 0.15 μm and 0.1 μm, respectively. In this case, scaling in $L_G$ beyond 0.1 μm does not improve $g_{m\_max}$ or $f_T$. In contrast, for the devices with a much shallower channel ($d_{QW}$ = 3 nm), $f_T$ can still increase as $L_G$ decreases, despite that $g_{m\_max}$ is still expected to reach a peak value of 530 mS/mm at $L_G$ = 0.15 μm as shown in Fig. 5. The reason that $g_{m\_max}$ peaks at a certain $L_G$ is mainly because of the 2-D effect, *i.e.*, DIBL. In another words, as $L_G$ shrinks, the gate essentially starts to lose control of the channel over to the drain. The effect of DIBL on threshold voltage, subthreshold slope and off-state leakage current is well known for silicon MOSFETs. However, the effect of DIBL on saturation transconductance has not obtained enough attention. This is because Si MOSFETs are mainly used for digital applications. Nevertheless, it has been reported in a simulation study of device scaling limits for silicon MOSFETs [7] that the saturation transconductance also peaks at a certain gate length if the vertical profile is fixed. On the other hand, the 2-D effect in the buried-channel MODFETs is more severe compared to surface channel MOSFETs. In addition, the source/drain series resistance aggravates the decline of the extrinsic transconductance as $L_G$ shrinks. Fig. 6 shows the simulated gate capacitance ($C_G$) vs. $L_G$ for the two sets of devices used in Fig. 4 and 5. Even though $C_G$ decreases monotonically with reducing $L_G$ for both sets of devices, the rate of $C_G$ decreasing depends on $d_{QW}$. For devices with $d_{QW}$ = 25.5 nm, $C_G$ decreases not as fast as $g_{m\_max}$ does, whereas for devices with $d_{QW}$ = 3 nm, $C_G$ decreases faster than $g_{m\_max}$ does. This explains why the peak $f_T$ starts to decrease for the devices with $d_{QW}$ = 25.5 nm at $L_G$ < 0.1 μm, while it keeps increasing for the devices with $d_{QW}$ = 3nm.

Fig. 7 shows that the DC voltage gain decreases rapidly for $L_G$ < 0.2 μm for devices with $d_{QW}$ = 25.5 nm due to increased output conductance, $g_d$, similar to the case of Si MOSFETs [7]. Furthermore, for fixed lateral dimensions and layer structure, reducing the source/drain junction depth, $X_j$, does improve voltage gain, even for the devices with $L_G$ = 0.1 μm, by suppressing bulk punchthrough and DIBL, as shown in Fig. 8. Hence, the vertical scaling of the layer structure is required for achieving higher $f_T$ and maintaining high voltage gain.

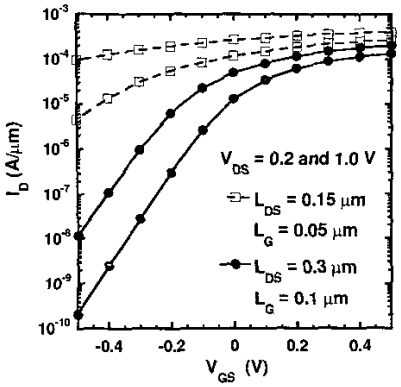


Fig. 3. Simulated $I_D$-$V_{GS}$ characteristics for two devices with the same layer structure and scaled $L_{DS}$ and $L_G$ ($d_{QW}$ = 25.5 nm, gate centered).

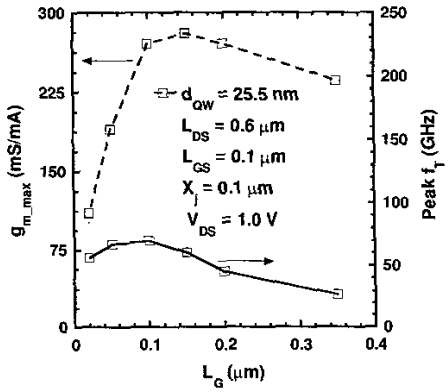


Fig. 4. Simulated $g_{m\_max}$ and peak $f_T$ vs. $L_G$ at $V_{DS}$ = 1.0 V for devices with deep quantum well channel and fixed $L_{DS}$ and $L_{GS}$ ($X_j$ = 0.1 μm).

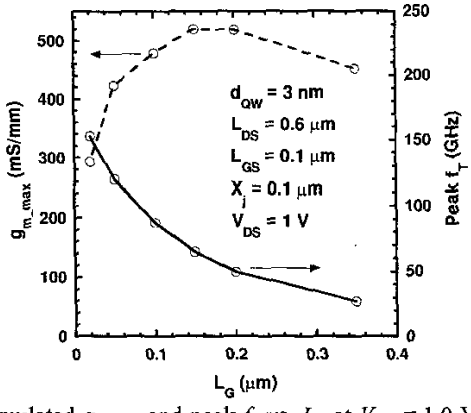


Fig. 5. Simulated $g_{m\_max}$ and peak $f_T$ vs. $L_G$ at $V_{DS}$ = 1.0 V for devices with a shallow quantum well channel and fixed $L_{DS}$ and $L_{GS}$ ($X_j$ = 0.1 μm).

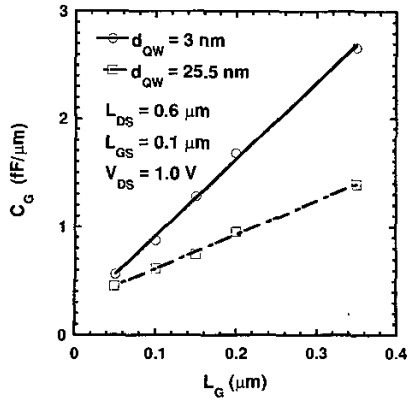


Fig. 6. Simulated $C_G$ at peak $f_T$ vs. $L_G$ at $V_{DS}$ = 1.0 V for two sets of devices as in Fig. 4 and 5.

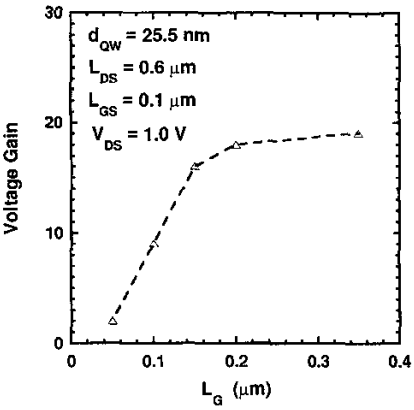


Fig. 7. Simulated DC voltage gain vs. $L_G$ for devices with $d_{QW}$ = 25.5 nm and fixed $L_{DS}$ and $L_{GS}$.

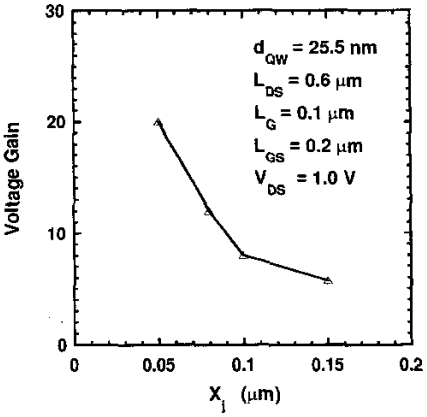


Fig. 8. Simulated voltage gain vs. $X_j$ for devices with $d_{QW}$ = 25.5 nm and fixed lateral dimensions.

The $L_{DS}$ dependence of the device performance for fixed $L_G$ and $L_{GS}$ is shown in Fig. 9. $f_T$ increases as $L_{DS}$ decreases due to reduced gate-to-drain series resistance, while the voltage gain decreases due to increased bulk punchthrough and DIBL. In order to maintain acceptable voltage gain for smaller $L_{DS}$, the source/drain junctions also have to be scaled accordingly.

The simulations also show that scaling $d_{QW}$ for fixed lateral dimensions ($L_G$ > 0.1 μm) will not enhance $f_T$ significantly. This is because not only $g_{m\_max}$, but also $C_G$ increases with reducing $d_{QW}$. However, if both lateral and vertical dimensions are scaled properly, significantly higher $f_T$ (>300 GHz) may be achieved with acceptable DC voltage gains (>10), as shown Fig. 10. It should be noted that for these MODFETs with good turn-on and turn-off characteristics, $f_T$ is approximately proportional to ($1/L_G$).

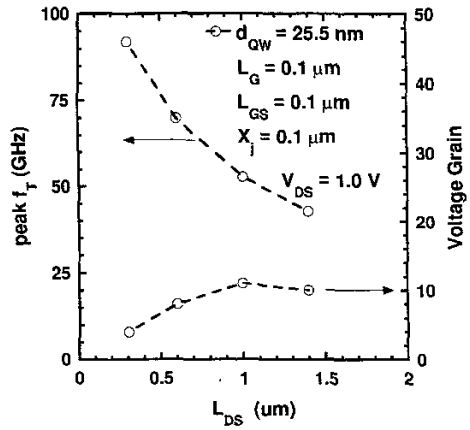


Fig. 9. Simulated peak $f_T$ and voltage gain vs. $L_{DS}$ at fixed $L_G$ and $L_{GS}$ ($X_j$ = 0.1 μm).

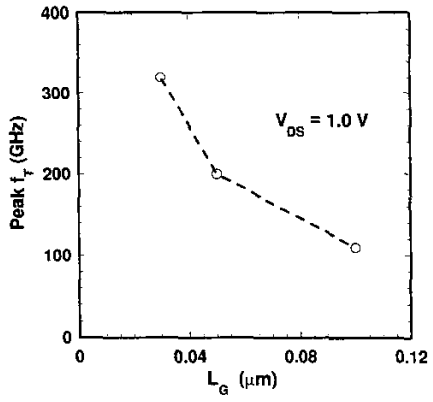


Fig. 10. Simulated peak $f_T$ vs. $L_G$ at $V_{DS}$ = 1.0 V for the devices with properly scaled lateral and vertical dimensions.

Preliminary experimental results have been obtained to confirm the trends reported in this paper. Si/SiGe nMODFETs have been fabricated on 200 mm wafers. The devices had $d_{QW}$ = 11 nm, $L_G$ ranging from 0.11 to 0.50 μm, and a variety of $L_{DS}$ and $L_{GS}$. Because the density of electrons in the quantum well was lower than intended, these devices have $f_T$ somewhat lower than anticipated. Nevertheless, the experimental results support the scaling trends reported above.

Fig. 11 shows the measured peak $f_T$ vs. $L_G$ at $V_{DS}$ = 1.0 V. For $L_G$ > 0.13 μm, $f_T$ is roughly proportional to $(1/L_G)$. However, at $L_G$ < 0.13 μm, $f_T$ starts to decrease for the devices with $L_{DS}$ = 1.0 μm, and begins to saturate for devices with $L_{DS}$ = 0.6 μm. The measured $g_{m\_max}$ also peaks at $L_G$ ~ 0.13 μm. These results confirm the simulation predictions that $g_m$ and $f_T$ do not scale with $L_G$ for the devices with deeply buried channels, but rather reach a maximum value at a certain $L_G$. Fig. 12 shows the measured DC voltage gain vs. $L_G$. The voltage gain decreases with reducing $L_G$ for fixed $L_{DS}$. It also decreases with reducing $L_{DS}$ for fixed $L_G$. These results confirm the simulation predictions that there is a tradeoff between higher $f_T$ and larger voltage gain. Measured devices with two different source/drain junction depths are also compared in Fig. 12. Higher voltage gain is achieved for the devices with a shallower source/drain.

## IV. Conclusions

Device simulations have been performed to investigate the scaling of Si/SiGe nMODFETs. Both DC and RF characteristics have been studied. Consistent with Dennard's scaling rule for silicon MOSFETs [8], it is found that in order to scale the MODFET performance, vertical scaling in the layer structure and source/drain junction depth is required, yet it is a fundamental challenge to maintain high mobility while decreasing the quantum well depth. The preliminary experimental results have confirmed the simulated geometric ($L_G$, $L_{DS}$ and $X_j$) dependences of the device performance for deeply buried quantum wells. Furthermore, the simulations indicate that, if better gate control is realized and short channel effects are suppressed, very high speed and large voltage gain can be achieved with properly scaled Si/SiGe nMODFETs. It should be noted that the extrinsic parasitics and the gate capacitance due to fringing fields from the non-zero gate height have not been included in this study of MODFET scaling. These effects will require additional device optimization and will be addressed at a later time.

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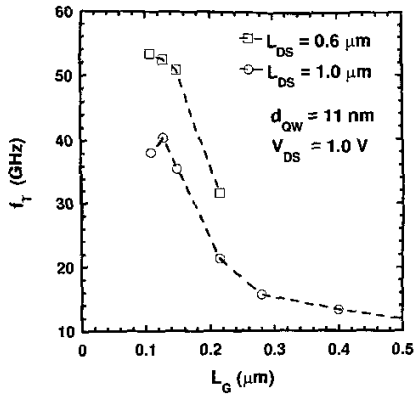


Fig. 11. Measured peak $f_T$ vs. $L_G$ at $V_{DS}$ = 1.0 V for device with $L_{DS}$ = 1.0 and 0.6 μm, and a deeper source/drain.

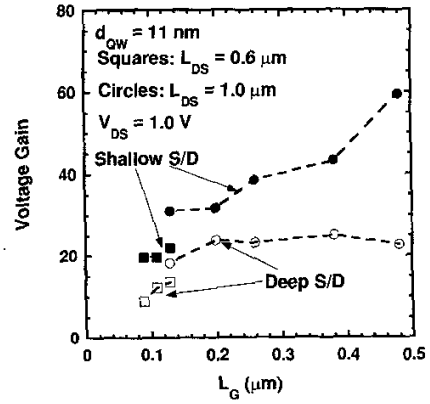


Fig. 12. Measured voltage gain vs. $L_G$ at $V_{DS}$ = 1.0 V for device with $L_{DS}$ = 1.0 and 0.6 μm, and two different $X_j$.

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