Circuit-Simulation Model of Gate-Drain-Capacitance Changes in Small-Size MOSFETs Due to High Channel-Field Gradients

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Abstract **- The field gradient along the MOSFET channel is included in the modeling of the gate-drain capacitance (C_{gd}) by an induced capacitance approach. The new approach has been successfully implemented in surface-potential based model HiSIM (Hiroshima-university STARC IGFET Model) and is capable of reproducing measured effects, which are particularly significant for pocket-implant technology, accurately.**

I. INTRODUCTION

RF applications of MOSFETs with gate lengths (L_g) in the 100nm regime are realistic not only due to MOSFET's low cost and high integration capabilities but mainly due to improved high frequency characteristics as shown in Fig. 1 [1]. For further improvement, it is desired that capacitances be reduced together with L_g. Among the gate capacitances, the C_{gd} contribution becomes increasingly important with scaling, since C_{gd} stays large in spite of the L_g reduction as demonstrated in Fig. 2. This is mainly attributed to the overlap and fringing capacitance contributions [2]. An additional contribution was attributed to the charge associated with the channel-side fringing field, later called the inner fringing capacitance. However, we have recognized that this contribution is negligibly small. For short-channel transistors, it has been shown that the velocity saturation affects the gate capacitances [3]. However, precise investigations are still missing.

In scaled MOSFETs, device characteristics are mostly determined by the field gradient near the drain, causing short-channel effects. This field is of course the origin of the velocity saturation. Working on measured C_{gd} and 2D simulations of small-size MOSFETs, we have found that the field gradient along the channel itself is an increasingly important factor which determines the C_{gd} value. Here we report an efficient surface-potential based MOSFET model of this effect for HiSIM [4]. In particular, the new C_{gd} model allows an accurate reproduction of measured C_{gd}-L_g characteristics for 100nm-scale MOSFETs with the pocket implant technology [5],[6]. Our investigation also predicts a reduction of C_{gd} with decreasing L_g due to the steep potential gradient introduced by the pocket implantation.

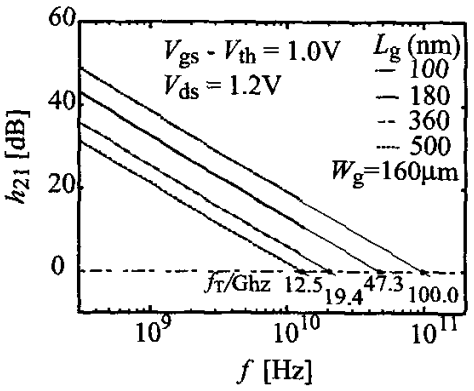

Fig. 1. Measured H-parameters (h_{21}) as a function of frequency (f) for a pocket-implant technology. The cut-off frequency (f_c) reaches 100 Ghz for a 100nm gate length MOSFET.

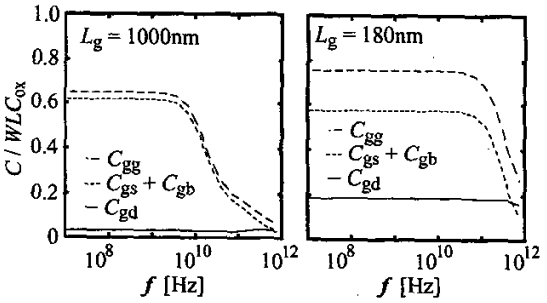

Fig. 2. MEDICI simulation of gate capacitances as a function of frequency (f), where C_{gg}=C_{gs}+C_{gb}+C_{gd}. C_{gd} remains significant at reduced L_g.

II. ANALYSIS OF 2D SIMULATION BY MEDICI

Generally, C_{gd} consists of two components: the intrinsic ($C_{gd,int}$) and the extrinsic ($C_{gd,ext}$) components,

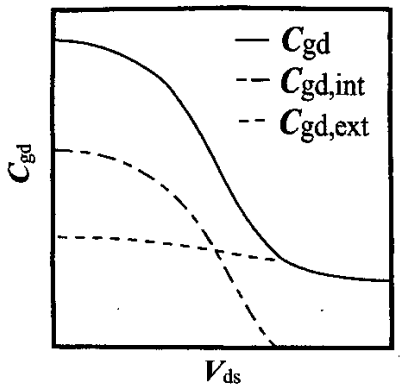

Fig. 3. Gate-drain capacitance components shown schematically. $C_{gd,ext}$ includes the overlap capacitance (C_{ov}) and the bias-independent outer-fringing capacitance (C_{of}).

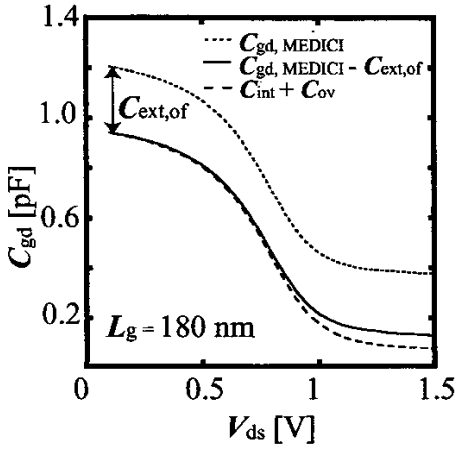

Fig. 4. Comparison of gate-drain capacitance calculated by MEDICI $C_{gd,MEDICI}$ and calculated by charge integration (C_{int}+C_{ov}). The difference is visible in the saturation region owing to high-field gradient. C_{of} is constant and bias-independent, and thus subtracted from $C_{gd,MEDICI}$.

schematically shown in Fig. 3. The intrinsic component is due to the mobile and depletion charges within the channel, while the extrinsic components include the overlap (C_{ov}) and the outer-fringing (C_{of}) capacitances. C_{ov} is bias-dependent and has been modeled separately [7]. Among the C_{gd} components, C_{of} is constant and bias-independent and thus can be neglected in the detailed simulation analysis. However, the sum of $C_{gd,int}$ + $C_{gd,ext}$ (= C_{ov} + C_{of}) alone is not sufficient to reproduce the total C_{gd}. The inclusion of an additional component coming from the charges induced by the field gradient is considered.

We have determined the field-gradient contribution to

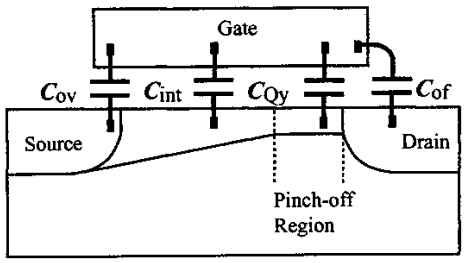

Fig. 5. The new C_{gd} model with C_{Qy} added to the conventional components.

C_{gd} in the following way. First, C_{gd} was simulated with the 2D device simulator MEDICI [8], which includes all inherent contributions. Then the intrinsic and extrinsic contributions to C_{gd} were calculated by integrating the charges as provided by MEDICI along the vertical direction first, and then along the lateral direction bounded by L_g. This integration thus includes all the bias-dependent components. A significant difference between these two C_{gd} calculations was found. The difference as shown in Fig. 4 is visible in the saturation C_{gd} which is explained by the lateral electric field (E_y) gradient along the channel. The space charge Q_y caused by the electric field gradient is calculated following

$$Q_y = \epsilon_{Si} w \int x_d(y) \frac{dE_y(y)}{dy} dy \qquad (1)$$

where w is the channel width, $x_d(y)$ is the depletion width and y is along the channel direction. The capacitance C_{Qy} due to this charge is given by C_{Qy}=dQ_y/dV, and is added to the conventional intrinsic and extrinsic components as shown in Fig. 5. The quantitative magnitude of C_{Qy} for L_g=180nm is demonstrated in Fig 6. As expected, this new C_{gd} component becomes important under the saturation region. More importantly in short-channel MOSFETs, E_y becomes appreciable and thus influences stronger. It is therefore necessary to include this new component into the circuit simulation of small-size MOSFETs.

III. SURFACE-POTENTIAL BASED MODELING

Since HiSIM is surface-potential based, having a quality-level comparable to a 2D device simulator, implementation of the proposed new C_{gd} model is straightforward. HiSIM knows all the potential values necessary to describe the induced capacitance, especially near the drain junction where the maximum lateral field occurs. The surface-potential distribution as described by HiSIM is shown in Fig. 7. By applying the Gauss law in the region where the lateral field steeply increases [9], Q_y is

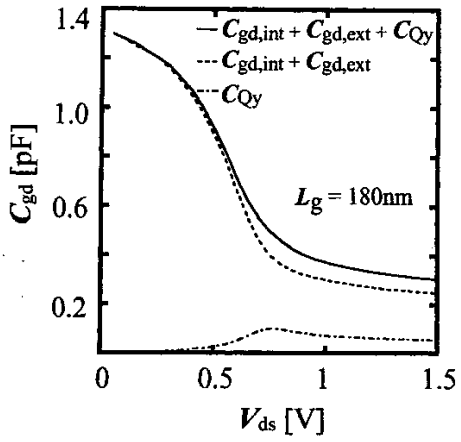

Fig. 6. $C_{gd,int}+C_{gd,ext}$ and C_{Qy} contributions to the gate-drain capacitance as simulated in MEDICI. C_{Qy} becomes significant in saturation C_{gd}.

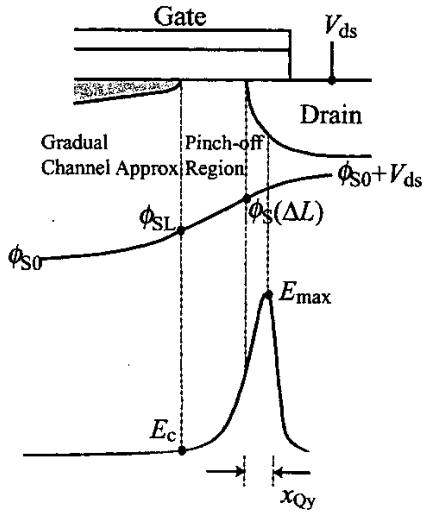

Fig. 7. Surface potential distribution of a MOSFET in saturation as modeled by HiSIM. Also depicted are the field points significant in C_{gd} modeling.

expressed as

$$Q_y = \epsilon_{Si} w x_d (E_{max} - E_c) \tag{2}$$

where

$$E_{max} = \frac{\phi_{s0} + V_{ds} - \phi_s(\Delta L)}{x_{Qy}}, \tag{3}$$

$\phi_{s0}+V_{ds}$ is the surface potential in the drain region,

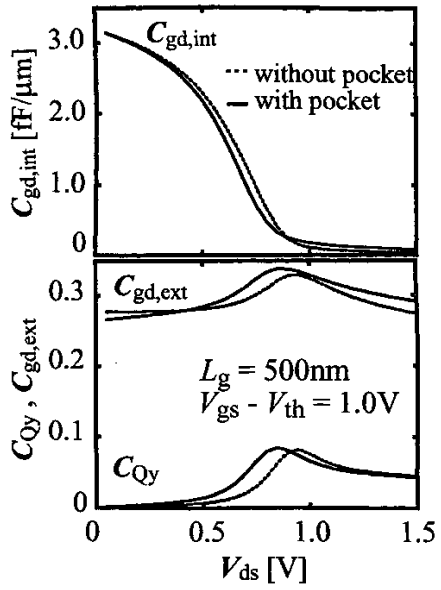

Fig. 8. Partitioned components of C_{gd} for pocket and non-pocket cases. In $C_{gd,ext}$ the outer-fringing capacitance is excluded.

$\phi_s(\Delta L)$ is the surface potential at the drain junction and E_c is the electric field at the end of the gradual channel approximation. A parameter (x_{Qy}), independent of L_g, is introduced indicating the position of the maximum lateral field from the drain junction. The induced capacitance C_{Qy} is then calculated as

$$C_{Qy} = \epsilon_{Si} w x_d \left(\frac{\frac{d\phi_{s0}}{dV_{ds}} + 1 - \frac{d\phi_s(\Delta L)}{dV_{ds}}}{x_{Qy}} - \frac{dE_c}{dV_{ds}} \right) \tag{4}$$

This induced capacitance is added to the conventional components as calculated by HiSIM.

IV. MODELING RESULTS FOR A 100nm POCKET-IMPLANT TECHNOLOGY AND DISCUSSION

Fig. 8 compares MEDICI simulation results of with and without pocket implantation for the different C_{gd} components. It is observed that the transition from the linear to the saturation region shifts to lower V_{ds} for the pocket-implantation case. This shift, which is true to all the components, is explained by the steeper potential increase of the pocket implant case near and in the drain contact as shown in Fig. 9. To achieve the same amount of high field for inducing this transition, a lower V_{ds} is thus sufficient for the pocket-implant case.

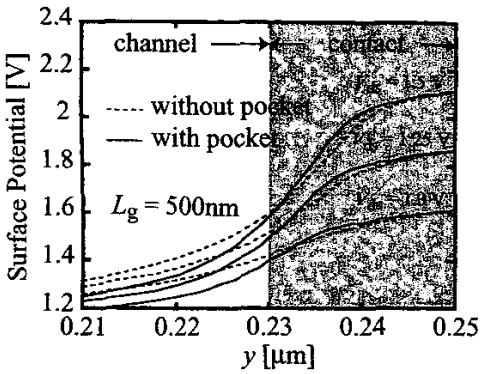

Fig. 9. Potential distribution for pocket and non-pocket cases. Pocket implantation results in steeper potential increase near the drain contact which extends into the overlap region.

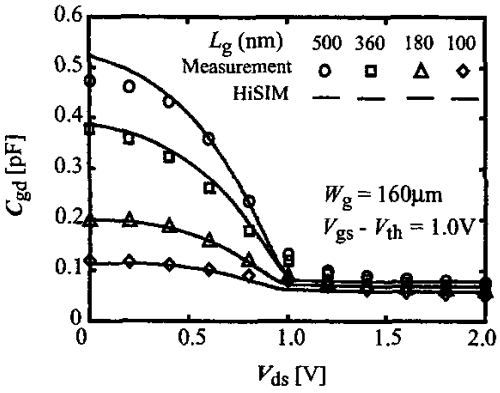

Fig. 10. HiSIM calculation for L_g = 500, 360, 180 and 100nm pocket-implanted MOSFETs in comparison to measurements.

Fig. 10 shows measured L_g-dependent C_{gd}-V_{ds} characteristics for a 100nm pocket-implant technology. Two important features, occuring for reduced L_g, are obvious:

- diminishing maximum at V_{ds}=0, and
- reduction of the saturation C_{gd}.

The physical reason for the diminishing maximum of C_{gd} with smaller L_g is the reduction of the relative size of the channel region in comparison to the pinch-off region, where Q_y is the main cause of the C_{gd} changes. At smaller L_g, the capacitance flattens because the magnitude of the saturation C_{gd} becomes comparable to that of the linear region. The physical reason for the C_{gd} reduction in the saturation region with smaller L_g is the shift of the beginning of the saturation region to lower V_{ds} due to the high lateral electric field near the drain.

Fig. 10 also depicts calculated C_{gd} by HiSIM using the new C_{gd} model. Since HiSIM models all features of the pocket technology on a surface-potential basis, good reproduction is achieved without needing any L_g dependent model parameters. Our results thus predict the positive effect of a reducing C_{gd} for future MOSFET-generations, owing to the high field near the drain, which was previously considered to be only undesirable.

V. CONCLUSION

We have developed a new C_{gd} model which includes the induced capacitance of the lateral field along the channel for small-size MOSFETs. The model, as implemented in HiSIM, achieves a good agreement with measured values down to L_g=100nm. The results promise reduced C_{gd} for pocket-implanted MOSFETs which is desirable in RF applications.

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