TCAD Driven Drain Engineering for Hot Carrier Reduction of 3.3V I/O PMOSFET

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Abstract – **We present a TCAD driven hot carrier reduction methodology of 3.3V I/O p-MOSFETs design. The drain structures are successfully optimized in short time by applications of TCAD local models. Considering tradeoffs between hot carrier injection (HCI) and I_{ON}, HALO/SDE of both core and I/O transistors can be totally optimized for photo-mask reduction.**

I. INTRODUCTION

Hot carrier-induced degradation in sub-micron pMOSFETs is serious concern. The reliability of surface channel core pMOSFET having thin gate oxide is often discussed [1]. But hot carrier injection (HCI) of 3.3V I/O pMOSFET also has a critical issue in case of having drain structure in common with core devices in order to reduce the process steps or photo-masks [2]. The process optimization is more complicated, therefore, TCAD driven process design is strongly required in industrial device development.
Although analysis of each pMOS HCI features have already reported, TCAD driven hot carrier reduction methodology is not much discussed. In this paper, 3.3V operation pMOSFET device design in view of both HCI immunity improvement and process step reduction is presented. TCAD driven optimization of SDE and HALO is the key of photo-mask reduction for surface channel pMOSFET design.

II. TCAD DRIVEN DRAIN ENGINEERING FOR HOT CARRIER REDUCTIN OF I/O PMOSFET

The mechanism of the degradation of device reliability in a pMOSFET is shown in Fig.1. The electron trapping is dominant due to drain avalanche hot carrier (DAHC) for $|V_{gs}| < |V_{ds}|$, while a hole trapping is dominant due to channel hot hole (CHH) for $|V_{gs}| \cong |V_{ds}|$. In 3.3V I/O transistor development, we focus on the HCI reduction optimizing SDE/halo in order to find the process windows in common with its core devices. Our optimization methodology is as follows (II-A, II-B).

A. TCAD Calibration Certifying SDE and HALO Dependence

For developing I/O transistor without extra process-steps and considering its hot carrier immunity, it requires to build well-calibrated local model which covers wide range of process parameters including core devices (Vt-dose, SDE dose, SDE energy and halo dose: Fig.2). The I/O's substrate current calibration is important for process optimization to evaluate DAHC component (Fig.3). Although the preliminary experiment for building TCAD local models cannot cover whole cross term of process parameters, TCAD helps the quantitative prediction including the cross term effect at the next drain engineering step.

B. I/O Drain Engineering for Hot Carrier Reduction and Common SDE/HALO with Core Devices

Complicated Vt-shifts are observed for $V_{gs}=V_{ds}/2$ stress bias (Fig.4). These are positive and negative Vt-shift due to electron and hole trapping, respectively. Usually hole trapping is severe but electron trapping induced initial Vt-shift can be problem. In order to reduce both electron and hole trapping at 3.3V I/O device which has the same drain structure as core device, drain engineering is required. The concept of the drain engineering is sub-surface Emax. (Fig.5). As Compared with shallow extension (SDE energy: $\leq$ 5keV, SDE dose: high), the peak of electric field (Emax) with optimized SDE (SDE energy: not low, SDE dose: not high $\sim 1 \times 10^{14} cm^{-2}$) is to be located at a sub-surface region below the Si/SiO_2 interface. Fig.6 shows simulated results of halo dose dependence of DAHC component. Fig.7 shows simulated results of SDE dose dependence of CHH component. As the results of optimization using by TCAD, the I_{ON} lowering of the optimized SDE compared to shallow extension case is within several percent (Fig.8: I/O and Fig.9:core). On the basis of this sub-surface Emax technique, we designed I/O drain structure in common with the core devices minimizing I_{ON} lowering of core devices and suppressing both DAHC and CHH of I/O devices.

III. DEVICE FABLICATION

Wafer processing mainly followed a general logic CMOS device. The channels of pMOSFET are doped by arsenic implantation after shallow trench isolation formation. The NO-treated dual gate oxides, 3.0nm for core and 7.0nm for I/O devices, are followed by un-doped poly-silicon deposition and gate patterning. Then, SDE/halo implantations for both core and I/O devices based on our TCAD driven optimization, side-wall spacer and deep source/drains are formed. Cobalt salicide process is applied to reduce the source/drain sheet resistance.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

Fig.10 shows measured halo dose dependence of positive Vt-shift caused by electron trapping (DAHC). Simulated halo dose dependence of electron injection rate (Fig.6) has strong correlation to measured Vt-shift. It is revealed that halo dose is the dominant factor to reduce the DAHC component. In view of CHH, SDE dose and energy are sensitive to Vt lifetime (ΔVt 50mV) (Fig.11). It is revealed that SDE condition is the key of HCI lifetime (CHH dominant) due to the reduction of lateral electric field or hole temperature (Fig.7). Experimental results of I_{ON} is shown in Fig.13 (I/O) and Fig.14 (core). These results agree well with TCAD predicted results (Fig.8 and Fig.9). The final results of our hot carrier reduction are shown in Fig.14 and Fig.15. As we expected, both DAHC and CHH components were successfully reduced. The HCI lifetime is also improved more than one order while maintaining both I_{ON}(core) and I_{ON}(I/O) ($\leq$several %) as a result of our methodology. The several percent lowering of drive current is acceptable to get the merit of photo-mask reduction except for high-performance logic.

V. CONCLUSION

We presented a TCAD driven hot carrier reduction methodology of 3.3V I/O pMOSFETs design. The drain structures are successfully optimized in short time by exhaustive applications of TCAD local models. The complicated cross term effects can be predictable. The presented methodology has general adaptability for the development of I/O transistor embedded in core logic. TCAD advantages specific to 3.3V I/O pMOSFETs design are as follows:

a) Considering the tradeoffs between HCI and I_{ON}, HALO/SDE of both core and I/O transistors can be totally optimized.

b) As the results of optimized common SDE/HALO conditions, we can reduce photo-masks maintaining the I_{ON} of core device.

REFERENCES

[1] N. Kimizuka, et al, Symp. VLSI Tech. P.73, 1999

[2] Y. Nishida, et al., IEDM Tech. Dig. T39_4, 2001

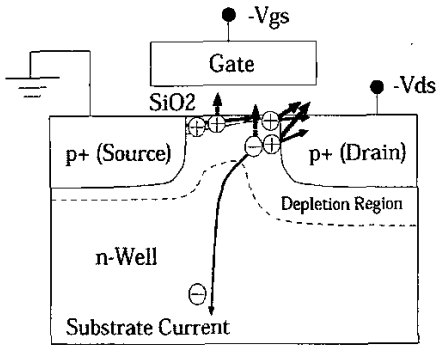


Fig.1. Schematic view of hot carrier-induced degradation in a pMOSFET. The electron trapping is dominant for |Vgs|<|Vds|. The hole trapping is severe for |Vgs|≥|Vds|.

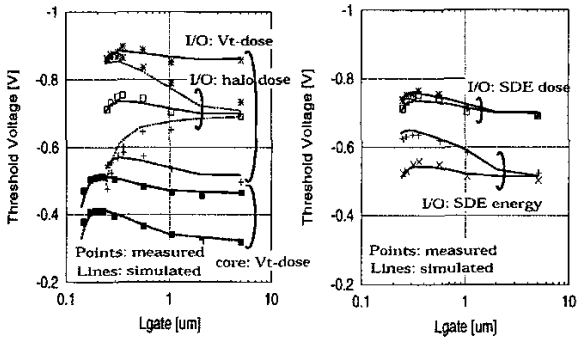


Fig.2. TCAD calibration results. For QTAT improvement of hot carrier immunity while maintaining target Vt, it requires to build the well-calibrated local model which covers 'wide range' of process parameters.

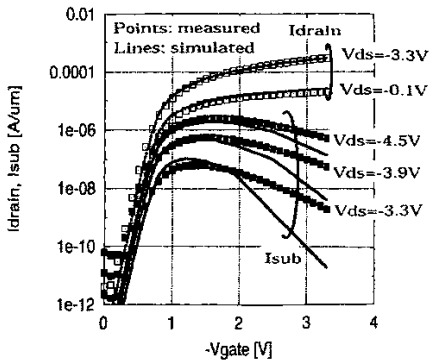


Fig.3. TCAD calibration results (I/O) of substrate current (Isub) caused by impact ionization(drift-diffusion & non-local impact ionization model).

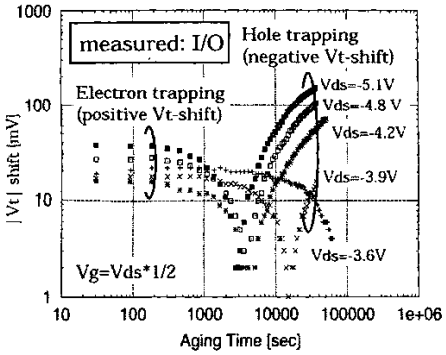


Fig.4. Measured Vt-shift (I/O) due to hot carrier degradation. In case of high Vds (@Vgs=Vds/2) stress bias, we find both positive and negative shift caused by electron and hole trapping, respectively.

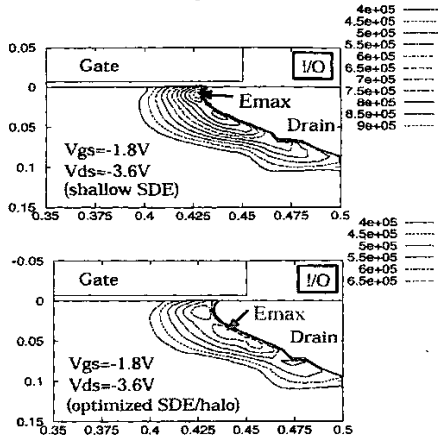


Fig.5. Electric field contours compared between shallow SDE and optimized SDE/halo (same Vt). We expected to reduce both drain avalanche hot carrier and channel hot hole.

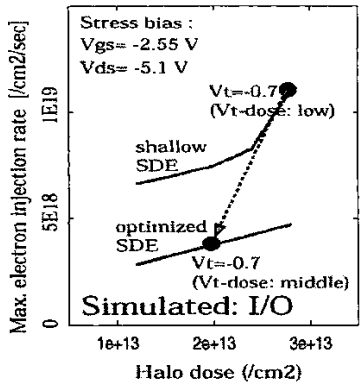
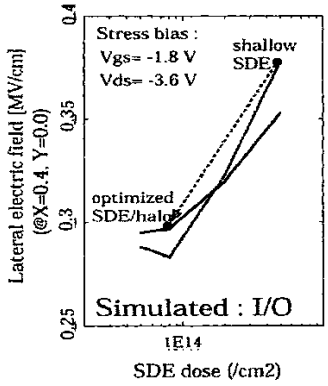
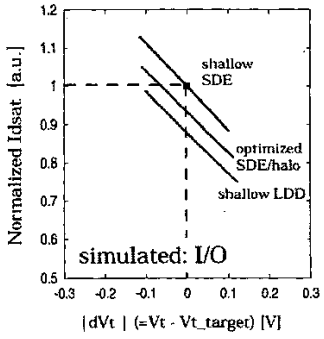


Fig.6. Simulated halo dose dependence of electron injection rate (lucky electron model). DAHC component is sensitive to halo dose and SDE energy.





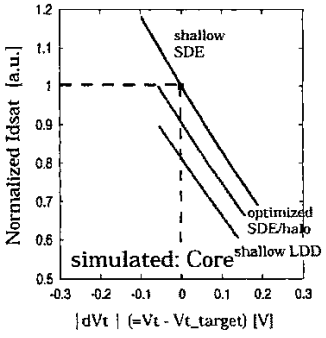


Fig.7. Simulated SDE dose dependence of lateral electric field (Ex). We used the Ex at 50nm inside from gate edge(drain side) for the first-order monitor of CHH.

Fig.8. and Fig.9. Simulated Vt versus Idsat of I/O(Fig.8) and core(Fig.9) devices compared between shallow SDE, optimized SDE/halo and shallow LDD (Vt-dose dependence).

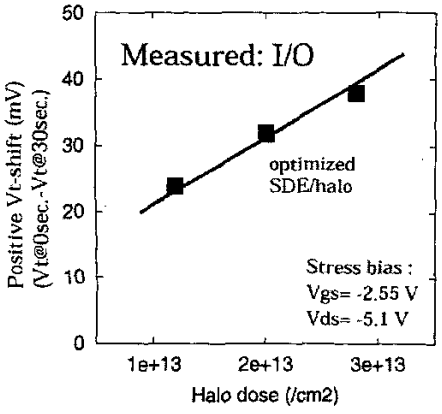


Fig.10. Measured halo dose dependence of positiveVt-shift caused by electron trapping (initial Vt=-0.7V). Halo dose dependence of electron injection rate by TCAD (Fig.6) agrees well with measured DAHC component.

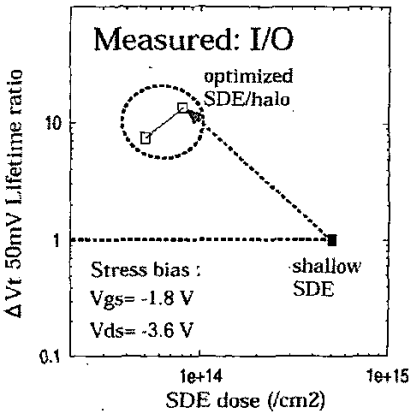


Fig.11. Measured SDE dose dependence of ΔVt lifetime. Simulated results (Fig.7) agree well with the tendency of CHH induced degradation component.

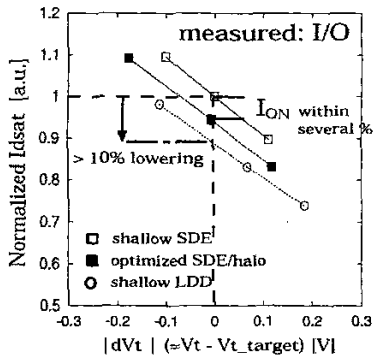


Fig.12. The merit of SDE/halo optimization. The I/O's Idsat lowering (matched Vt) is within several percent while reducing HCI.

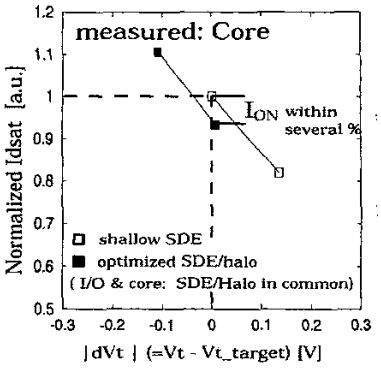


Fig.13. The core's Idsat lowering (matched Vt) is within several percent in case of using the same SDE/halo as I/O device.

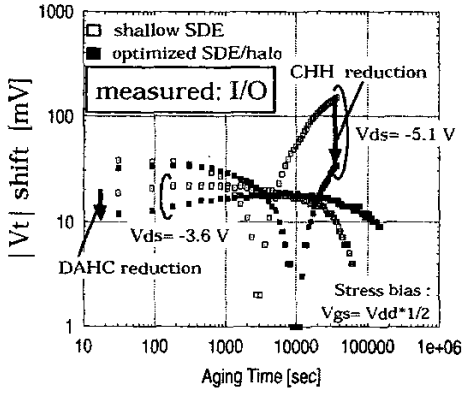


Fig.14. Experimental results of hot carrier reduction. As we expected, both DAHC and CHH components were reduced.

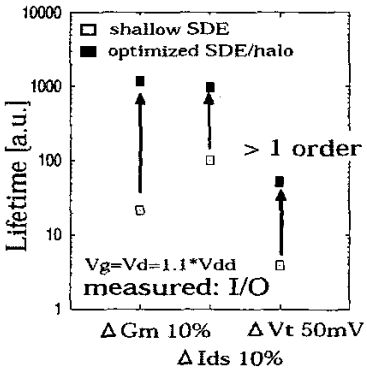


Fig.15. HCI lifetime of 3.3V I/O pMOSFET at Vg=Vd=1.1*Vdd stress. We successfully improved lifetime more than one order.