GIDL Simulation and Optimization for 0.13μm/1.5V Low Power CMOS Transistor Design

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Abstract – **In this work, we calibrate a BTBT model based on measured GIDL data, and incorporate the model into our process/device simulations to directly correlate process with device performance and leakage. For the first time, we quantitatively explore an overall picture of tradeoffs between device leakage and performance as functions of process conditions. The explored design space has been used in process optimization for our 0.13μm/1.5V low power (LP) CMOS transistors. We demonstrate that such predictive TCAD simulations to determine and optimize process conditions can effectively reduce development time and cost. We describe GIDL mechanisms in our 0.13μm/1.5V LP transistors, and explain, via simulations, that the measured GIDL current manifests different I-V behaviors depending on whether the dominant BTBT location is at the gate oxide/Si interface or below in the Si bulk.**

I. Introduction

As technology scales from sub-0.25μm into sub-0.1μm, stand-by leakage control and the tradeoffs with device performance have been the major concerns in low power (LP) CMOS transistor design. As high channel (halo) doping levels are used to control sub-threshold leakage (Ioffs), diode leakage currents become non-negligible (Fig.1) [1-3]. In particular, in sub-0.25μm LP devices, the Gate Induced Drain (or Diode) leakage (GIDL) due to the band-to-band tunneling (BTBT) at the gate oxide/Si interface (or in Si bulk) need to be suppressed to sub-pA/μm range through process optimization [1,3].

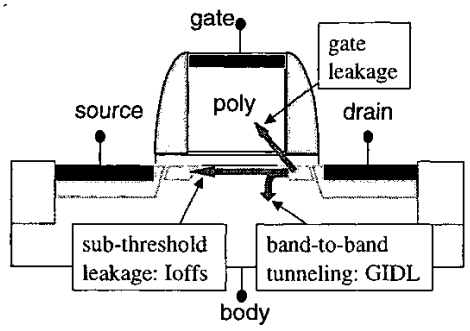


Fig.1: Typical leakage currents in a modern silicon based bulk transistor. Total leakage, Ioffd, is collected at the drain.

Previous work on GIDL has been focused on either the BTBT theories [4-6] or device simulations to match I-V data [4,7]. In this work, we calibrate a BTBT model based on experimental GIDL data, and incorporate the model into our well-calibrated process/device simulator based on TSUPREM and MEDICI. Our process/device simulations directly correlate process with device performance and leakage. For the first time, we quantitatively explore an overall picture of tradeoffs among Ioffs, GIDL, Ioffd (drain leakage), and Idrive (drive current) as functions of process conditions. The explored design space has been used in process optimization for our 0.13μm/1.5V LP CMOS transistors. We demonstrate that such predictive TCAD simulations to determine and optimize process conditions can effectively reduce development time and cost. We describe GIDL mechanisms in our LP transistors, and explain, via simulations, that the measured GIDL current manifests different I-V behaviors depending on whether the dominant BTBT location is at the gate oxide/Si interface or below in the Si bulk.

II. BTBT Mechanisms and GIDL Simulation

The BTBT has three major contributing mechanisms: (a) phonon-assisted direct tunneling, (b) midgap trap-assisted tunneling, and (c) midgap trap-assisted tunneling combined with thermal emission (Fig.2). Minority carriers emitted due to the tunneling are removed to the substrate, majority carriers are collected at the drain as the GIDL current. The BTBT current density J, either through direct or trap-assistance involved tunneling, can be equivalently formulated as a function of electric field (E-field) E

$$J \propto E^{\alpha} \exp(-\beta/E), \qquad [1]$$

where α = 2-2.5, determined by the bandgap type: either direct or indirect [5,6], and β is ~ 10^7 V/cm.

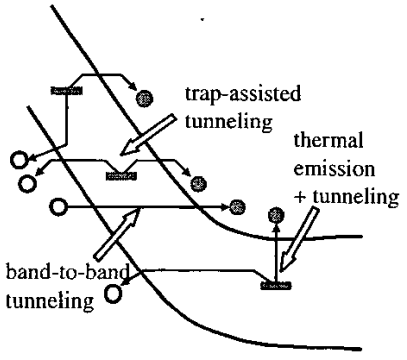
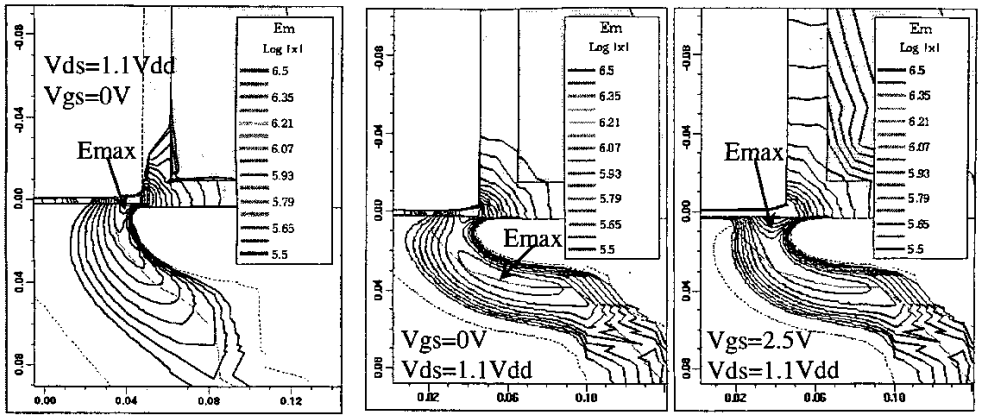


Fig.2: Various mechanisms can contribute to GIDL current. Horizontal transitions are tunneling, and vertical are thermal emission, respectively.

The 2-D electric field (E-field) distribution has been simulated for our representative 0.13μm/1.5V LP NMOS & PMOS transistors (Fig.3). When the transistors are at off-status (V_{GS} = 0V) with the drain biased at 1.1V_{DD}, a high E-

field region exists near the drain. For the NMOS, the peak E-field is at the gate oxide/Si interface. The vertical component of the surface E-field at the dominant tunneling point has strong influence on GIDL current [7]. Fig.4 shows that the NMOS GIDL increases by over 100x when V_{DG} is increased by 0.5V. In contrast, for the PMOS, the peak E-field is located ~ 350A below the interface. Thus, the vertical E-field has limited impact on GIDL. The PMOS GIDL increases only 1.2x by the same V_{DG} increase of 0.5V (Fig.4). The simulated GIDL shows a two-regime dependence on V_{DG}. For V_{DG} at 1.0V or above, the PMOS



(a) NMOS (b) PMOS

Fig.3: E-field magnitude contours. At Vgs=0V, the peak E-field in bulk is located at the interface for NMOS, while for PMOS, it is located at a sub-surface region ~ 350A below the interface. Increase Vgs to accumulation (2.5V), the PMOS peak E-field shifts to the interface.

enters the surface E-field dominant regime, where vertical E-field has a strong impact on GIDL. Fig.3(b) shows the simulated E-field magnitude contours for the PMOS at two V_G biases. Note that the dominant BTBT point shifts from sub-surface to the gate oxide/Si interface with increasing V_{DG} (Fig.5).

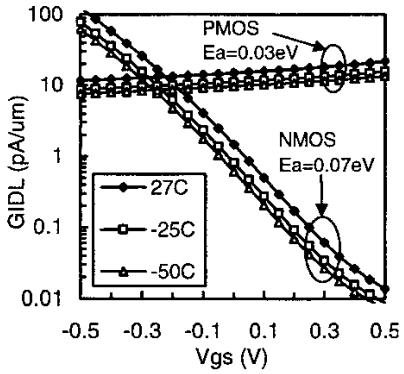


Fig.4: Measured GIDL current at Vds = $1.1V_{DD}$ for Vgs from –0.5V to +0.5V, at temperatures of 27C, -25C, and –50C.

Phonon-assisted direct tunneling probability is very low due to the indirect bandgap of silicon. The midgap trap-assisted BTBT is the major source for GIDL. In Fig.4, GIDL increases 1.5-2.5x for both NMOS and PMOS with temperature from –50C to 27C. Compared to the impact by V_{DG}, thermal emission from midgap traps plays a minor role for the NMOS [5]. The thermal emission activation energy Ea is extracted at V_{GS} =0V through Arrhenius fitting (Fig.4).

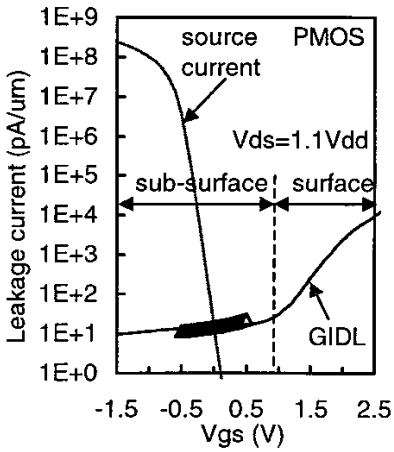


Fig.5: PMOS I-V curves show BTBT point transition from sub-surface to surface with Vgs increase. Simulation matches experimental data (Δ) at 27C.

III. Device Optimization

Reducing both peak E-field and implant damage related midgap traps through the optimization of implant energy, dose, and anneal is key to reducing GIDL. Deep level traps caused by implant damage and salicidation, such as B-, P-, As-, Sb-related defect pairs, Si_i-clusters, and 3*d*-transition metal (Ni, Co, Cu) involved defects [8, 9], can be reduced through optimization of pre-amorphization, halo and MDD implant conditions, as well as anneal recipes. For LP devices, low halo and MDD dose combinations are chosen

to reduce E-field and junction abruptness, thus to suppress GIDL caused by trap-assisted BTBT.

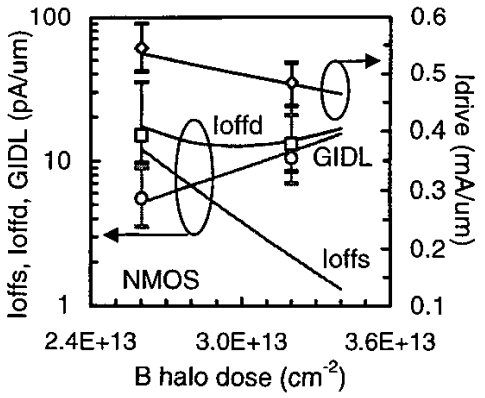


Fig.6: NMOS halo design: Idrive, GIDL, Ioffs, and Ioffd as functions of B halo dose at a fixed MDD and VT condition.

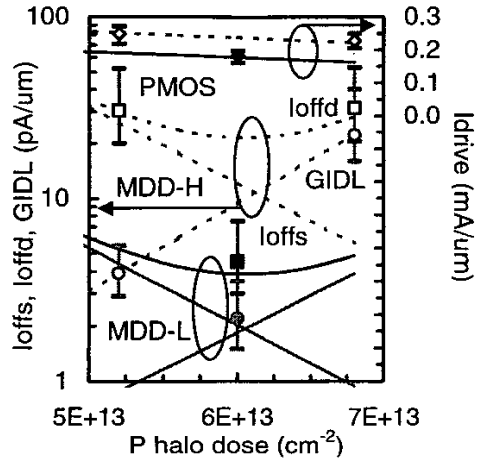


Fig.7: PMOS halo and MDD: Idrive, GIDL, Ioffs, and Ioffd variation with P halo dose at high (MDD-H) and low (MDD-L) MDD dose conditions.

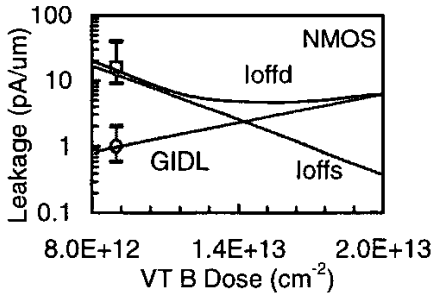


Fig.8: NMOS VT implant design: GIDL, Ioffs, and Ioffd as functions of VT B dose at fixed halo and MDD conditions.

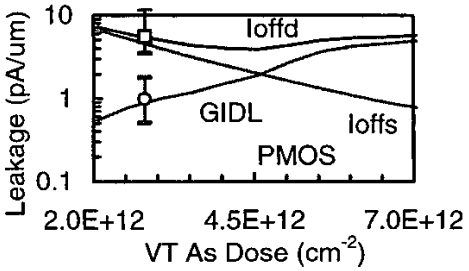


Fig.9: PMOS VT implant design: GIDL, Ioffs, and Ioffd as functions of VT As dose at fixed halo and MDD conditions.

Fig.6 (NMOS) and Fig.7 (PMOS) show several simulated curves with measured data of GIDL, Ioffs, Ioffd, and Idrive as functions of halo and MDD doses. GIDL increases with both halo and MDD doses, and become the major leakage component at high dose cases. Total leakage (Ioffd) reaches its minimum at certain halo and MDD doses. The tradeoffs between leakage and Idrive are used to construct design contours to search process conditions for optimal device performance. Leakage currents (Ioffs, GIDL, and Ioffd) exhibit similar dependence on channel implant dose (Figs.8 & 9). GIDL increases with VT dose at fixed halo and MDD conditions.

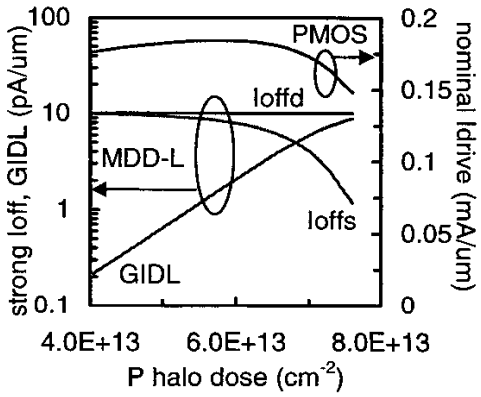


Fig.10: A PMOS RSM based on TCAD to identify halo dose for optimal Idrive along 10pA/um Ioffd contour at 6keV BF2 MDD.

Fig.10 shows PMOS design contours as an example. Even for a well-controlled robust process, gate length varies in a certain range around Lgnom, the targeted nominal gate length. Lgmin and Lgmax are the lower and upper 3σ limits for gate length variation. Process conditions can be found for low GIDL and optimal Idrive along strong Ioffd = 10pA/μm (the upper limit at Lgmin) contour generated from a response surface model (RSM) based on TCAD simulations. Our 0.13μm/1.5V LP transistor design features 2.6nm physical gate oxide and ~ 0.1μm nominal gate length. Based on this TCAD optimization, we successfully achieved GIDL reduction over 5-15x to ~ 1.0pA/μm, low Ioffd, while maintaining high Idrive in only two development stages of our 0.13μm/1.5V LP CMOS transistors (Fig.11).

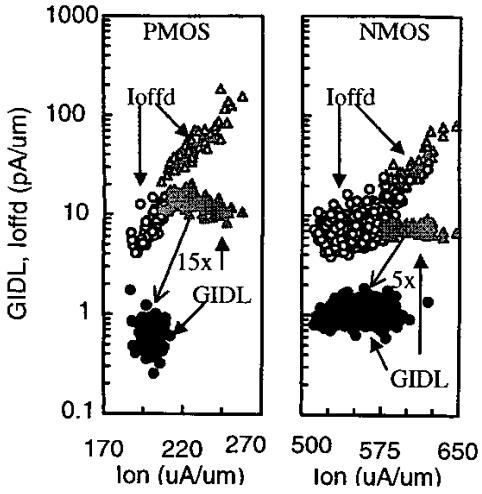


Fig.11: TCAD process optimization to reduce GIDL over 5-15x, to achieve total leakage control and device performance.

IV. Summary

We incorporated GIDL in our simulations to identify process conditions for the optimal tradeoffs between device leakage (GIDL, Ioffs, and Ioffd) and performance (Idrive) for our 0.13μm/1.5V LP transistors. We demonstrated that such predictive simulations to determine process conditions can effectively reduce development time and cost. We discussed BTBT mechanisms and explained related GIDL I-V features. As technology scales into sub-0.1μm, the methodology described in this paper will play an important role in realizing efficient design optimization, especially in suppressing GIDL (or diode leakage) caused by trap-assisted BTBT in LP bulk CMOS transistors.

Acknowledgments

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