1-2 (Plenary)

Integrated TCAD and ECAD Solutions – A Paradigm Shift

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Abstract – **This paper highlights the emerging need for selective integration of physical-model based TCAD modeling and simulation tools that have been mostly applied to technology development with ECAD tools that have been traditionally used for product design. The emerging technology trends that lead to this paradigm shift are highlighted. The architecture and requirements of integrated TCAD-ECAD solutions are also discussed along with the infrastructure required to successfully meet this challenge.**

I. INTRODUCTION

Nearly four decades ago, Gummel [1] suggested a self-consistent numerical scheme for solving the partial differential equations that govern the physical operation of 1D bipolar transistors. Shortly after, this work was extended and applied to p-n junctions [2], IMPATT diodes [3], and junction field-effect transistors [4]. These work represent the beginning of TCAD in numerical device modeling. Pioneering work on silicon process modeling started a decade later [5-7]. The geometry and material composition of devices from process modeling have directly aided the device and process engineers in their work and used in combination with device simulators to model device's electrical characteristics. Another major milestone in TCAD modeling was the advent of lithography modeling in the late 1970's [8,9]. It provided physical simulation of features in lithography patterning. An enormous amount of research has been performed during the subsequent 20-30 years on physical models, numerical techniques, model calibration and software implementation, and has transformed TCAD modeling in device, process and lithography into mainstream tools for processing technology development. The scope of TCAD modeling has also expanded to new areas such as equipment modeling, process reliability, manufacturing control, etc.

While tremendous strides have been made, TCAD R&D in both universities and industry should be maintained and expanded to meet the challenges in the development and manufacturing of nanometer processing technologies. Furthermore, the targets of processing technology and the definitions of product are increasingly coupled while product design must also comprehend increasingly more technology features. TCAD researchers should look beyond processing technology and explore new opportunities where TCAD modeling can make major impacts on product design for improved accuracy, reduced margins, and minimum rework.

II. TECHNOLOGY TRENDS WITH MAJOR IMPLICATIONS ON PRODUCT DESIGN

Four technology trends that have important implications on products and therefore product design requirements are discussed: (1) strongly coupled technology targets and product definitions, (2) scaling and exponentially increasing transistor density, (3) interconnect system with increasing operating frequency, coupling and complexity, and (4) process variations of random and systematic origins.

Setting appropriate targets is one of the earliest and most important tasks in the life cycle of any given processing technology and it will have profound effects on products during their entire life span. In any given product, there exist many different logic and analog circuits that have different population and different impact on product's overall performance. The use of simple metrics such as I_{DSAT} and $C_{GATE}V_{CC}/I_{DSAT}$ as the sole performance targets of a processing technology has become increasingly insufficient. Reduced supply voltage and increased short channel effects in transistors have amplified this insufficiency. To further complicate the matter, different products may have different requirements, such as frequency and power.

The exponentially increasing transistor density as predicted by Moore's Law (Fig. 1) in conjunction with increasing transistor leakage and product frequency has many consequences for products, and increased chip power dissipation is one of the major concerns. Higher power consumption generally leads to increased chip temperature, which impacts both product performance and reliability. In chip design, maximum temperature calculated from worst-case power consumption has normally been applied to performance analysis and electromigration assessment. However, power density is non-uniform across the chip (Fig. 2). This results in transistors of the same size at different locations having different performances and wires of the same size at different locations having different allowed currents. To support aggressive product design, the non-uniform temperature distribution on the die and in the multi-layer interconnect system must be incorporated into the EDA design solution. However, to obtain an accurate temperature distribution, the tool must be able to comprehend from the layout the complex 3D interconnect structures, the density and distribution of devices and metal wires as well as properties of composite materials, and perform heat transfer analysis.

It is becoming more frequent when empirical, rule-based ECAD tools and methodologies can not

accurately extract the capacitances and resistances of on-chip interconnects due to the scaling of interconnect wire size and spacing, increased number of metal layers, complexity in 2D and 3D structures, and multi-layer composite dielectric materials (Fig. 3). Reduced supply voltage and GHz chip operating have brought forth two additional issues that are critical to signal integrity and timing, namely the cross-coupling capacitances and on-chip inductances. Accurate analysis of the impact of noise due to cross-coupling capacitances requires much improved RC extraction. The modeling and extraction of on-chip inductance, a non-local physical effect, is very complex and of large scale in nature. One of the key challenges in inductance modeling is the determination of the current return path in a complex metal system, an extremely difficult if not impossible task a priori to exhaustive 2D/3D full-wave simulations. Illustrates in Fig. 4 is an application of full-wave solution to the analysis and design of a large-scale bus system. Intuitively the current return path is expected to be the neighboring parallel metal lines. However, rigorous full-wave simulation showed significant current returned through the near-by orthogonal metal lines as a consequence of the displacement current. This finding is critical to the design of a high quality bus system. In a complementary role to high-capacity EDA solutions, TCAD modeling ranging from analytical to full-wave simulation can be applied to the modeling of strategically selected domains of the interconnect system, depending on the criticality and complexity.

Products are designed under considerable uncertainties from both process variation and final circuit operating conditions [10]. These uncertainties have been largely accounted for by guardband margins and worst-case design. However, it has become more difficult to simultaneously meet the performance and the yield targets using this approach, and a strong need for more accurate estimation of these uncertainties has emerged. Three general sources of uncertainty that affect circuit design are shown in Fig. 5, and the focus here will be the third source of uncertainty which encompasses process changes and drift, process control, systematic and random variations, etc. Process variations interact strongly with the other types of uncertainties. Only a few years ago most of the process variability was attributed to die-to-die and wafer-to-wafer variations. Due to aggressive scaling of transistor and limitations of manufacturing equipment, within-die variation arising from spatial variations in wafer processing has become dominant [11-13]. Examples are lens aberrations and reticle variations on line widths, pad pressure variations on the thickness of post-polishing layers, and non-uniformities in implantation on device doping concentrations. These within-die variations result in properties of devices and interconnect wires to be dependent on dimensions, location in the reticle field, orientation with respect to the stepper lens, and proximity to neighboring structures, etc. Shown in Fig. 6 is a lithography simulation of non-uniform distribution of the background light intensity caused by optical flare [14]. This directly impacts the final sizes of devices and metal lines that have strong implications on product performance and reliability.

III. INTEGRATED TCAD-ECAD SOLUTION

Figure 7 illustrates the scope and the hierarchy of TCAD modeling. SPICE models and circuit simulation have been traditionally the main linkages between processing technology and product design. They provide the most accurate description of wafer implementation of circuits and the critical role in characterizing ECAD models and simulators of higher order abstraction for faster simulation and analysis required in very large-scale designs.

While measurement data are traditionally used to characterize SPICE models, the use of TCAD simulation to represent nominal "data" has been on the rise, particularly during the pre-silicon or early development stages when measured data are unavailable and an early start on product design is required [15]. More recently, TCAD simulation has also been applied to the characterization of skew-corner model files to include the effects of process drift and process control, and assist the definition of processing technology targets [15].

Although the application of TCAD modeling in characterization of nominal and skew SPICE model files and definition of technology targets has increased, several major improvements are needed to better support product design. Model predictability is the most fundamental driving force behind TCAD modeling. This is particularly important in applications such as the setting of processing technology targets and pre-silicon SPICE model file characterization that are of the most importance to product design. R&D on enhancing model predictability in all domains of TCAD should be continued and accelerated. However, two additional areas requiring focused efforts should be noted: (1) module-level integration among TCAD modeling tools and (2) selected integration of TCAD modeling tools at layout-level and on platforms consistent with ECAD.

The potential benefit of module-level integration is illustrated by the TCAD system shown in Fig. 8. The system can be applied to assist the setting of the targets of processing technology. This integrated system ha built-in predictive device simulation, automated SPICE model characterization, a circuit simulator containing the characterized SPICE models, a built-in optimizer, and sets of circuits where each set is representative of the performance of a major product. This system can be applied to tune the process technology for a particular product. It can also provide "data" on short-range process variations that resulted from causes such as implant variation for SPICE skew-corner model file characterization.

The need for improved layout-level integration is illustrated in Fig. 7. As an example, the lack of couplings between CMP and the interconnect simulator modules will prevent the inclusion of one important source of process variation in the characterization of skew-corner SPICE interconnect model files. The lack

of coupling at the layout-level between the lithography and the process modeling modules will, on the other hand, prevent the generation of more accurate chip-location dependent SPICE model files that are highly useful in critical path timing analysis and chip-level leakage power analysis.

The final deficiency to be pointed out is the lack of consistency among the layout databases employed. This is conceptually illustrated by the lines of different colors that are connecting TCAD modeling modules to the "Layout Data & Processing" module as shown in Fig. 7. This deficiency will seriously limit the potential leverage of all of TCAD modeling tools by ECAD solutions that are unified for performance verifications and reliability verifications. These include power/thermal analysis for performance and reliability, RC extraction for timing analysis, RC extraction for electromigration analysis, and full-chip inductance extraction for signal integrity analysis, etc.

The discussion has been focused on TCAD portion of the integrated TCAD-ECAD solution. There are other requirements in building complete, integrated TCAD-ECAD solutions.

IV. REQUIRED INFRASTRUCTURE

Successful development of integrated TCAD and ECAD tools and solutions that comprehend these emergent processing technology trends for product design has some key infrastructure requirements. An extended partnership of CAD developers with process technologists and product designers is essential. Design solution strongly depends on the design problem at hand, the features and latitudes of the processing technology, the targets in product performance and reliability, and the interaction between technology features and product. A clear understanding of these issues is essential to developing CAD solutions that address real issues and are optimized for trade-off between accuracy, performance and other requirements.

TCAD developers usually are physics, process and modeling oriented, and experienced in models and tools that are at the physical level. TCAD tools and solutions in general have close mappings to parameters of processing technology, and have wider range of predictability. ECAD developers are usually software and computer science specialists, and experienced in high performance tools and solutions and integration with high-level design flows to address large-scale design problems. ECAD solutions are often abstractions of physical problems with processing technology contents significantly simplified or reduced. Integrated TCAD-ECAD solutions that address the aforementioned technology trends for design require a team with a combined TCAD-ECAD expertise and an integration strategy with coordinated roadmaps.

To quickly provide solutions to meet the rapidly changing tool requirements, the software should be modules and libraries with well-defined interfaces to allow wide reuse and rapid integration. Modular software components with standardized interfaces also provide the flexibility and opportunity for solutions that are based on mixing proprietary and vendor tools.

V. SUMMARY

The complexities in processing technology and product resulting from processing technology scaling, increased density and operating frequency of devices and multi-layer interconnects, decreased supply voltage, and systematic and non-systematic process variations that include layout-dependencies, are increasing at an accelerating pace. Improved integration among TCAD modeling areas and selective integration of TCAD and ECAD solutions are becoming increasingly critical in assisting optimum product design with aggressive design margin and minimum re-work. To achieve this goal, it requires concerted and integrated efforts among technologists, product designers and developers of TCAD and ECAD solutions.

ACKNOWLEDGEMENT

The author wishes to acknowledge members of the TCAD Division for their work that are represented in this paper.

REFERENCES

[1] H.K. Gummel, *IEEE Trans. Electron Devices*, vol. 11, p. 455 (1964)
[2] A. DeMari, *Solid-State Electron.*, vol. 11, p. 33 (1968)
[3] D.L. Scharfetter and H.K. Gummel, *IEEE Trans. Electron Devices*, vol. 16, p. 64 (1969)
[4] D.P. Kennedy and R.R. O'Brien, *IBM J. Res. Dev.*, vol. 13, p. 662 (1969)
[5] D.A. Antoniadis, S.E. Hansen and R.W. Dutton, *Report 5019-2, Stanford University* (1978)
[6] D.A. Antoniadis and R.W. Dutton, *IEEE J. Solid State Circuits*, vol. 14, p. 412 (1979)
[7] H. Ryssel et al., *IEEE Trans. Electron Devices*, vol. 27, p. 1484 (1980)
[8] W.G. Oldham et al., *IEEE Trans. Electron Devices*, vol. 26, p. 717 (1979)
[9] W.G. Oldham et al., *IEEE Trans. Electron Devices*, vol. 27, p. 1455 (1980)
[10] S. Duvall, Proc. Intl. Workshop on Statistical *Metrology Workshop*, p. 56 (2000)
[11] H.S. Wong and Y. Taur, *IEDM*, p. 705 (1993)
[12] P. Oldiges et al., *Int. Conf. SISPAD*, p. 131 (2000)
[13] S. Nassif, *Proc. Statistical Metrology Workshop*, p. 2 (2000)
[14] C. Krautschik et al., *Proceedings of SPIE*, vol. 4688, p. 289 (2002)
[15] C. McAndrew, *International Conference on Simulation of Semiconductor Processes and Devices*, p. 12 (2000)

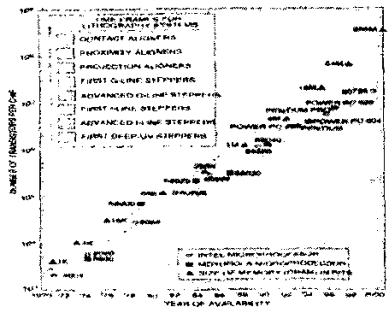

Fig. 1 Moore's Law on transistors density (Source: Scientific American)

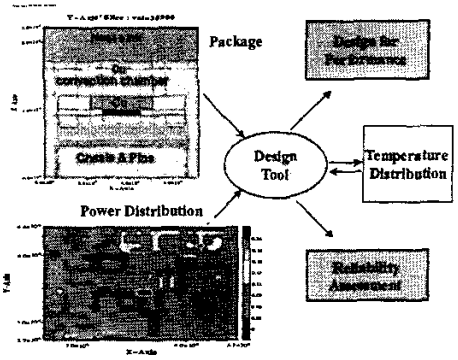

Fig. 2 Accurate temperature analysis requires power distribution and detailed physical structures

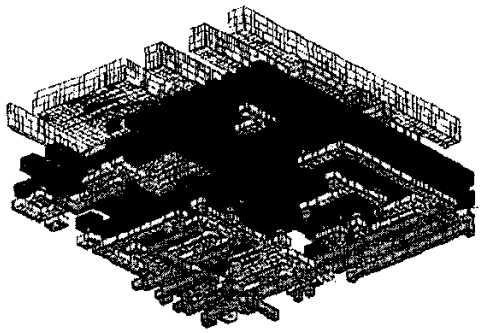

Fig. 3 Complex on-chip interconnect system

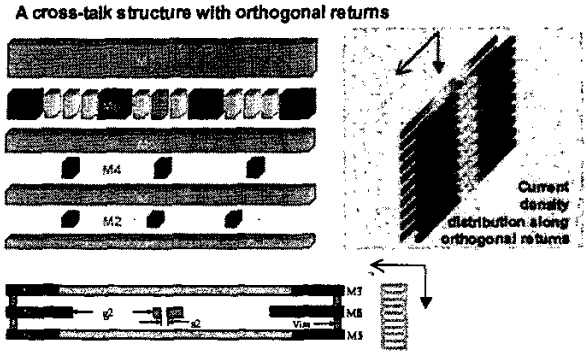

Fig. 4 Full wave simulation for return path determination fin a large-scale bus system

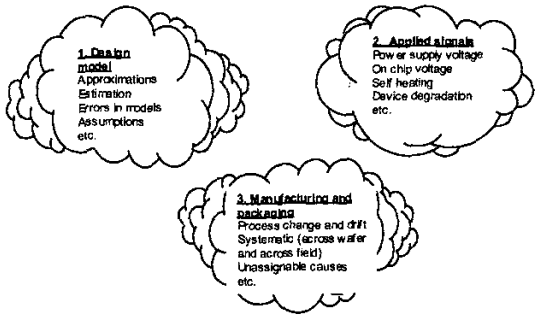

Fig. 5 Three general sources of uncertainty that affect product design

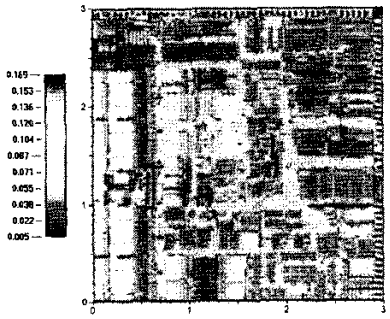

Fig. 6 Non-uniform background light intensity caused by optical flare that directly impact final feature sizes

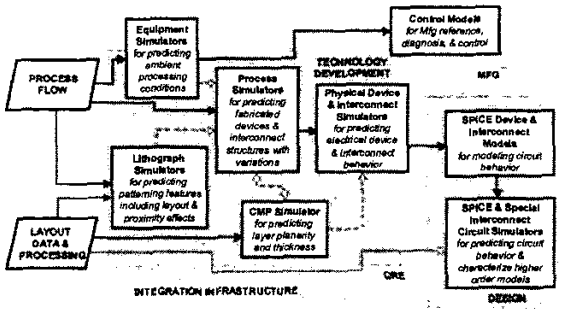

Fig. 7 Hierarchical TCAD modeling system

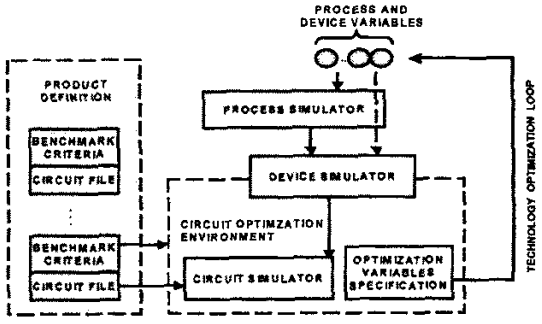

Fig. 8 System for assessing processing technology targets based on product specific requirements