A Practical CMP Profile Model for LSI Design Application

Toshiyuki Ohta*, Takeshi Toda and Hisasi Ueno**
NEC ULSI Device Development Lab., **VLSI Manufacturing Engineering Division
1120 Simokuzawa, Sagamihara, Kanagawa 229-1198, Japan

Abstract

We have developed a practical CMP model. The model is based on the elastic mechanics. For the practical use, some numerical treatments including a new time iteration method are developed. Using the model, numerical errors in a test chip are reduced to less than 1% with 5 minutes EWS calculation time. The simulated results well agree with experiments within 5% errors.

Introduction

As the integration of LSI progress, multi-layer process has become more important. The short-range flatness has been improved by CMP(Chemical-Mechanical-Polishing) process. But long-range flatness still remains, which causes the capacitance difference and the reduction of the focus margin in the lithography process. To improve these effects, simulation models have been developed with the accurate model with the contact analysis[1], and some simplified models for fast calculation [2][3]. We think the former model is too costly to apply to design and the latter models are insufficient to apply to LSI design practically as to the speed and precision including numerical errors. So in order to establish a practical model, we have improved the model and developed some treatments and a new time iteration control method. Then we applied the model to a test chip and compared with the experiments. Finally we show some approaches to reduce the long-range uniformity.

Model

1.Assumption

CMP profiles are modeled using the following assumption. The stress put on the pad, which is reverse proportional to the pattern density, is calculated considering one dimensional stress balance and stress response with the neighboring regions by pad deformation using the elastic mechanical theory. Polishing rate is calculated with the stress by Preston's equation.

*Now he belongs to Semiconductor Leading Edge Technologies, Inc., 292 Yoshida-cho, Totsuka-ku, Yokohama,244-0817,Japan
Tel:+81-45-866-6763 Fax:+81-866-6879
E-Mail: ohta@selete.co.jp

2.Simulation Procedure

As the CMP profile simulation, the distribution of the upper oxide pattern height (hi) as shown in Fig.1 is calculated against the polishing time with the following procedure. Block diagram of the simulation system is shown in Fig.2.

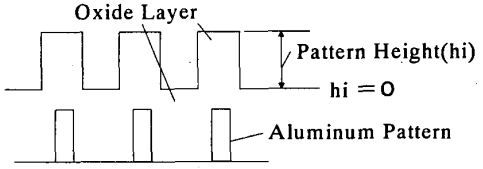

Fig.1 The schematics of CMP profile

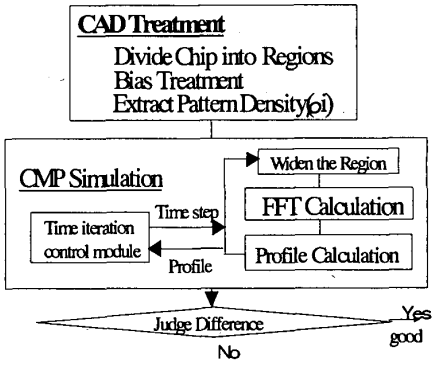

Fig.2 Block diagram of CMP simulation system

(1) A chip region is divided into several regions.
(2) Pattern density of each region is calculated with a CAD tool taking pattern bias into account.
(3) In i-th region whose pattern density is ρi, and whose average oxide height is hi, polishing depth(Δhi) for a time step(Δt) is calculated with the equation

$$\Delta hi = A\Delta t[E/l\{hi - FFT^{-1}\{FFT(h)*FFT(f(x))\} - Po\}/\rho i \quad \ldots(1)$$

where E is the elastic constant and A is a constant, l is the thickness, Po is a given pressure, and f(x) is a stress response function, and FFT means the fast Fourier transform.

(4) The stress response function f(x) is extracted from the normal stress in the pad surface, which is calculated by axis-symmetrical elastic stress analysis (with ANSYS) on the condition that displacement of the central point of the pad is fixed.

(5)In the vicinity of large pad, the gap between pad and device is important. For the strict calculation, the contact stress analysis is used [1]. In this model the contact problem is approximately modeled by keeping the polishing velocity positive ($\Delta hi/\Delta t > 0$).

3. Numerical treatments

The pattern density wavers by the region division. Especially in the extremely small pattern density region happening to originate in the region division, calculated pattern height in the first time step of equation (1) becomes extremely small negative value ($hi << 0$). But actually, polishing rate decreases abruptly if the pattern height is negative, so pattern height is almost 0. Therefore large random errors are generated. To improve the random errors, we developed such a treatment that if polishing depth in a step is larger than the height of the previous step, the height is settled to 0 and the density is set to 1 in the region.

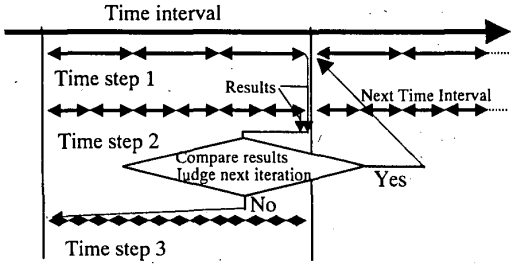

Fig.3 Schematic diagram of time iteration control method

The oxides film thickness in the CMP process is calculated by the equation (1) using the forward Euler's method. So to reduce numerical errors, the time steps must be very small. Besides, CMP polishing rates are strongly dependent on the previous profiles.

To reduce the calculation time, we have developed a new time iteration control method as shown in Fig.3. The CMP profiles are calculated repeating with two different calculation time steps in a fixed interval. Analyzing the results, the time step of the next interval is determined. If necessary, the profiles of the same interval are recalculated with finer time steps.

Results and Discussions

Using this model, the simulated polishing profiles of a test sample chip were compared with the experiments. In experiment the samples were fabricated as the following process. Plasma CVD oxide films were deposited on the patterned aluminum films on the silicon substrates. The oxide films were polished with a CMP apparatus. Residual film thickness was measured with laser beam. The chip size is 15mm×15mm and the chip region is divided into 128 × 128 regions in the simulation. Mask-patterns used in the test chip are shown in Fig.4.

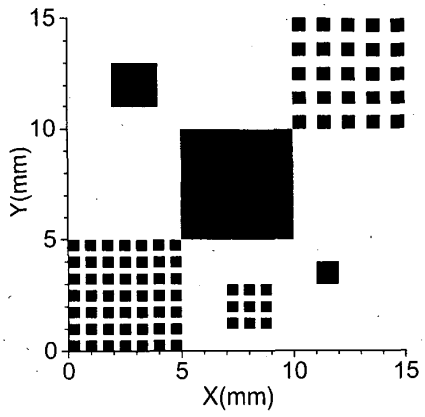

Fig.4 Photo-mask pattern of test chip

This chip includes a large aluminum pad. So this chip is useful for the examination of the way to reduce long-range height difference.

1.Accuracy and speed

Fig.5 shows the relation between the profile calculation time using EWS(SPECfp95=8) and

the maximum numerical errors in the chip changing the time step as a parameter. The errors are calculated as the maximum difference from an accurate calculation result in the chip. It is found the effect of time iteration control method is not only that the time steps are adjusted automatically but also that using this method, time discretizing errors are reduced by 20% compared with the errors with most suitable constant time steps. With a calculation time schedule with Δt=12sec iterating 15 times and Δt=6sec iterating 30 times, the computation time is within 5min* and numerical errors is less than 0.005 microns (< 1%). These results imply that this model is practical enough for application to LSI design.

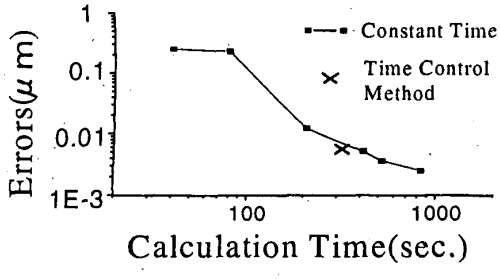

Fig.5 Numerical errors vs. calculation time: Performance with time iteration control method compared with constant time step is shown.

2.Comparison with experiments

Simulated results of residual film thickness dependence on polishing time in the several points of the test chip are compared with experiments. Fig.6 shows the results simulated and measured in the medium of large aluminum patterns with the size of 1mm, 2mm, and 5mm square. Fig.7 shows the results in the medium pad of pattern arrays with the pattern density of 30%, 50%, 100%. Simulated and experimental profiles in a cross-section of the large (5mm square) aluminum pad at several time steps are shown in Fig.8.

From these results, simulation results well agree with experiments within 5% errors.

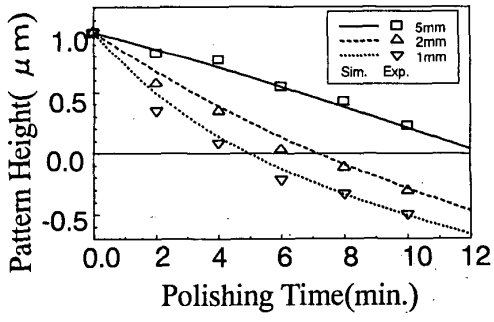

Fig.6 Comparison of simulation with experiment: Parameter is pattern width(1,2,5mm) in the test chip.

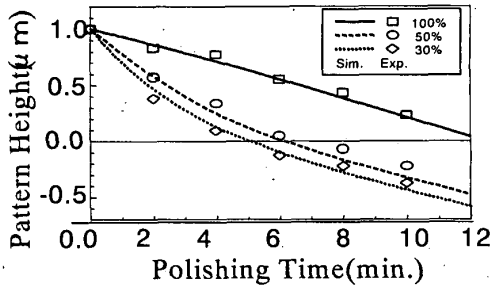

Fig.7 Comparison of simulation with experiment: Parameter is pattern densities(30.50.100%) in the test chip.

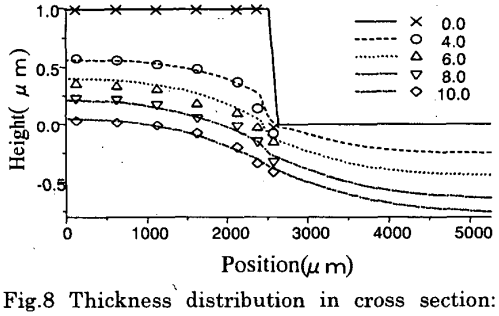

Fig.8 Thickness distribution in cross section: Simulation results compared with experiments

3. 3D profiles and applications

Fig.9 shows the simulated 3D profiles at polishing time of 2 and 8 minutes. The pattern difference generated in the first stage in the polishing is found to diminish as the polishing progresses. The long-range height difference (max-min in the chip) is 0.66 microns at the polishing time of 8 minutes.

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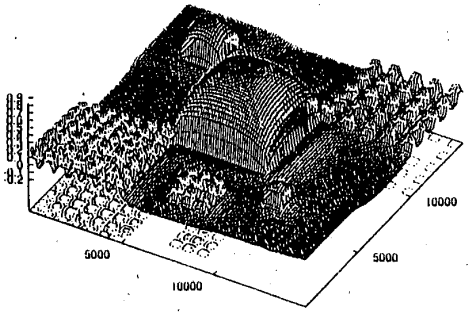
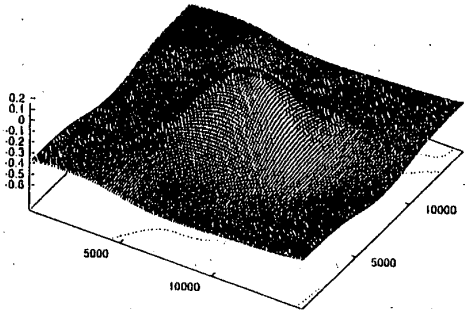
* In the explanation, please be careful lest you confuse the calculation time with the polishing time



Polishing time is 2 minutes



Polishing time is 8 minutes

Fig.9 3D profile simulation results at the polishing time of 2 and 8 minutes.

Finally, we show two results how to improve the long-range height difference. Fig.10 shows a profile calculated when the elastic constant is 10 times as large as used in Fig.9. The height difference is improved to 0.22 microns but still remains. Fig.11 shows a profile calculated for the chip, when dummy aluminum patterns with the size of 104 microns square are added in the medium of every region whose pattern density is 0. (With this treatment, uniformity of pattern density of the regions is improved.) The height difference is improved to 0.23 microns.

The model we have developed here can be applied to LSI design by using together with LSI verification tools.

Conclusion

We have developed a practical model for CMP profiles. Using the model numerical errors are reduced to less than 1% with 5 minutes calculation time with EWS. The simulated results well agree with experiments within 5% errors. This model is applied to LSI design and gives the solutions to realize long-range flatness.

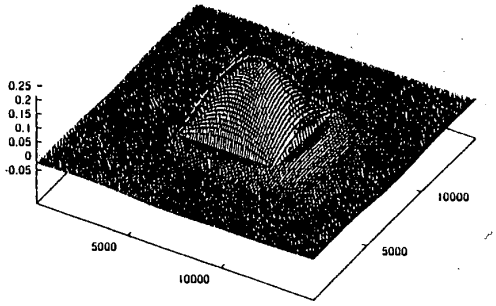


Fig.10 3D profile simulation results with hard CMP pad

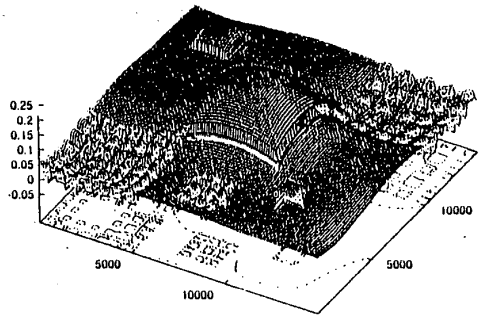


Fig.11 3D profile simulation results with setting 104 micron square dummy pattrn.

References

[1] Y-H.Kim et. Al 1997 SISPAD Proc. Pp.69-72

[2] D.Ouma et. Al.., Digest of IITC-98 pp.67-69

[3] T.-L.Tang,1997 SISPAD Proc. Pp.65-68