ELECTROMAGNETIC SIMULATION FOR THE MODELING OF INTERCONNECTS

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Modeling of interconnects and packaging plays a key role in modern microelectronic circuits for many reasons which are convergent from an advanced system and economical point of view but antagonist from a physical or electromagnetic one :

For modern VLSI circuits the well known Moore's law is used to generate road maps describing the expectations for the next generations of integrated circuits in which downsizing is accompanied by increasing circuit complexity and increased die size. This will greatly affects clock speed, interconnects and wire length as illustrated figure 1 [1]. Modern VLSI chips are expected to operate with a 1 GHz clock frequency at the end of this century with a corresponding wire length exceeding 1 km per chip.

Modern telecommunication systems will require the processing of extreme high bit rates and signal frequencies (≥20 Gbits/S or 20 GHz) while allowing a technological compatibility with low-end frequencies down to 0 Hz.

In modern radar systems (as well as in telecommunication systems) digital and mixed mode multichip modules (MCM) are used which combine GaAs MMICs and Silicon control devices to perform a desired function. In such a mixed mode environment with analog and digital functions operated in close proximity, advanced interconnect and packaging play a key role.

It is clear that modern electronic systems need to design more functionality into less space which can be achieved for example by a three-dimensional circuit and packaging approach based on integrated circuit assembled into layers with effective connections between the layers. However frequency dependent electromagnetic parasitic effects such as dispersion, ohmic losses, parasitic coupling and radiation can heavily deteriorate the electrical performance and lead to costly and time-consuming design cycles if modern corresponding design tools are not developed.

With this evolution of complex modern mixed mode circuits and subsystems the traditional rivalry between GaAs and Si technologies must stop and complementary contributions must be searched from both sides, GaAs softwares being more developed to account for high frequency phenomena and Si base platforms more suited for large scale integration. None of them however can respond to-day to the pressing need of advanced interconnect modeling which needs new concepts at fundamental levels of circuit design and diagnostics.

But interconnect is a wide concept and in order to clarify the problem according to figure 2 [2], we shall distinguish three levels of interconnection :

- On chip interconnect and chip interconnection
- Report substrate and associated technology
- Packaging

To characterize interconnections and analyse packaging effects, a variety of electromagnetic models has been developed using either time or frequency techniques.

Depending on the ratio of the wavelength over the circuit critical size ($\lambda g/l$) different approaches can be considered :

1. $\lambda g/l >> 1$. In this case, the line method can be used.
2. $\lambda g/l \cong 1$. The Maxwell equations have to be solved with various possible degrees of approximation.
3. $\lambda g/l << 1$. Asymptotic methods based on the diffraction theory can be used.

With the increasing speed and the reduced size of modern circuits case 2 where the wavelength is of the same order of magnitude as the circuit size is coming the most frequent situation which needs a solution of the Maxwell equations.

Some powerful frequency and time domain techniques have been already established :

- Frequency-Domain Integral Equation Method
- Frequency-Domain Finite Element Method
- Finite-Difference Time-Domain Method
- Finite-Difference Frequency Domain Method

These various techniques will be briefly described and their ability to handle frequency dependent behaviour of substrate materials (loss especially) will be discussed.

Results derived by these techniques on various kinds of interconnects will be presented and accuracy along with computational efficiency will be compared and discussed. Examples will be chosen in the field of digital, RF and microwave monolithic or hybrid circuits and modules.

This paper will conclude on the present state of interconnect CAD tools and on the necessary and most urgent improvements to be achieved in that field.

<u>References</u> :

[1] Scaling theory in modern VLSI ', D.K Ferry and L.A. Akers, Circuits & Devices, Sept.97.

[2] Advanced process and manufacturing technologies for microwave/MMV modules, E. Feurer, B. Hou, M. Oppermann, 1997 IEEE MTT-S Workshop on « Low-cost millimeter wave products : design and manufacturing issues ».