Integrated Three-Dimensional Topography Simulation and its Application to Dual-Damascene Processing

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Abstract

A completely three-dimensional (3D) simulation of the processes involved in the fabrication of a dual-damascene (DD) interconnect scheme has been carried out. For the simulations, an integrated 3D topography simulator has been used which comprises modules for the 3D simulation of optical lithography, etching, and layer deposition. The sputter deposition of TiN is investigated in more detail by means of simulation. As no re-emission of metal atoms from the surface is assumed, no simulation parameters are necessary and the only input required is the geometry of the feature and the sputter reactor. It is shown that for the DD structure considered here collimated sputtering does not result in sufficient step coverage and therefore chemical vapor deposition (CVD) is required for TiN barrier deposition.

1. Introduction

With decreasing feature sizes of integrated circuits, interconnect wiring gains more and more impact on resulting performance. Therefore, new interconnect schemes are being developed, such as dual-damascene (DD) architecture which we investigate in this paper by means of completely three-dimensional (3D) topography simulation.

A topography simulator, called SC-TOP, has been developed which is capable of simulating 3D surface evolution during optical lithography (for planar and non-planar substrates), etching, and layer deposition using the simulation modules SOLID-C, MASTER, and DEP3D, respectively. Features that have now been implemented include lithography on non-planar substrates, different wet- and dry-etching processes, low-pressure chemical vapor deposition (LPCVD), and conventional as well as collimated and long-throw sputter deposition. The simulation of the topography process steps is performed by using one graphical user interface which allows the specification of topography process sequences and process parameters for the individual steps and which also ensures smooth data transfer between the different modules. The simulator is part of a suite of 3D process simulation modules developed within the European project PROMPT [1].

In this paper, we show the 3D simulation of the entire process sequence and investigate in more detail the deposition process of the TiN barrier layer, which is crucial for the reliability of copper interconnections.

2. 3D Simulation of Dual-Damascene Processing

To realize a DD interconnection scheme, different approaches can be taken [2]. The sequence we consider here consists of the following process steps: On top of the planar substrate, a 0.5 μm thick oxide layer is deposited by plasma enhanced chemical vapor deposition (PECDV). A 0.2 μm thick SiN layer is deposited by PECVD. The SiN layer is then structured using a lithography step followed by an etching step. Holes are opened in the SiN layer at the positions where the contact holes will be etched in the oxide. The simulated geometry is shown in Fig. 1. The next step is PECVD of a 0.5 μm thick oxide layer. The following lithography step generates a resist profile with the pattern of the interconnecting lines. A dry-etching step with a high selectivity between oxide and SiN (in the simulation assumed to be 30) results in both the trenches for the interconnecting lines and the contact holes to the substrate. Metallization to fill the contact holes and lines is performed by CVD (e.g. with a metal-organic precursor [3]) of a 0.1 μm thick TiN layer followed by a copper layer of 1.2 μm thickness. Both deposition steps are assumed to yield a conformal layer profile as it has been observed in experiments [3]. Planarization is performed by chemical mechanical polishing (CMP) which has been simulated by specifying a completely anisotropic etching step. The geometry of the lines and contacts is shown in Fig. 2. A cross sectional view is presented in Fig. 3.

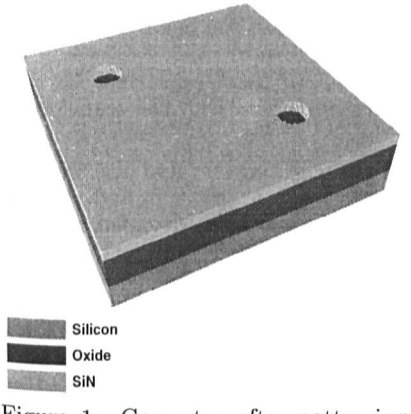

Figure 1: Geometry after patterning the SiN layer at the contact hole positions.

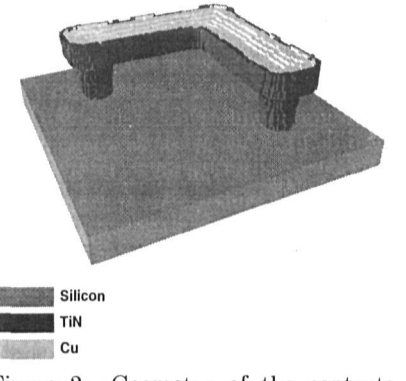

Figure 2: Geometry of the contacts with interconnecting lines. The oxide and nitride layers are not shown.

3. Evaluation of PVD and CVD Methods for Barrier Deposition by Means of Simulation

Sufficient step coverage of the barrier layer (in our example a TiN layer) is essential for the reliability of the integrated circuit. For all positions at the contact hole or trench surface the thickness of the layer must be large enough to provide an effective

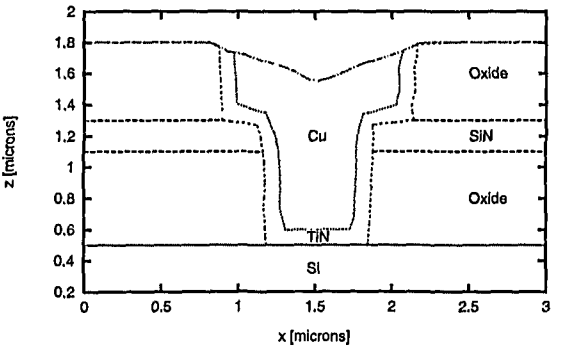

Figure 3: Cross section through the middle of one of the contact holes.

barrier against diffusion of copper atoms into the silicon or oxide. Today, physical vapor deposition (PVD), e.g. sputter deposition, is the common method used for barrier deposition. However, with increasing aspect ratios of contact holes and vias, PVD does not yield sufficient step coverage, even if techniques such as collimated sputtering or ionized metal plasma (IMP) deposition are used. Therefore, a shift towards CVD processes may be necessary in the future.

In this paper, we demonstrate how simulations can be used to check in advance whether a specific PVD process is suitable to obtain sufficient step coverage of a barrier layer. The PVD process we consider here is collimated reactive sputter deposition of TiN. We assume an isotropic emission of atoms from the sputter target and an operating pressure low enough to yield a mean free path far larger than the distance between sputter target and substrate. In consequence, the metal atoms move along straight lines on their way from the target to the substrate. Proceeding on the assumption that the metal atoms are not re-emitted from the surface, no free parameters remain and the layer shape is completely determined by the geometry of the feature, the reactor, and the collimator.

For the simulation of the sputtering process, the target diameter and the distance between target and substrate were set to typical values, i.e. 300 mm and 50 mm, respectively. The position and the aspect ratio of the collimator were varied to study the influence on the layer conformality. The parameter having the strongest influence on the layer shape is the collimator aspect ratio. A trade-off between bottom coverage and sidewall coverage can be observed. With increasing collimator aspect ratio bottom coverage is improved, however at the expense of reduced sidewall coverage. The best conformality was found for a collimator aspect ratio of 1 (a square grid collimator was assumed), a position of the collimator very close to the substrate (i.e. the ratio of the distance between the bottom side of the collimator and the substrate to the collimator height is 0.1), and a position of the DD structure beneath the location where the collimator vanes cross. For these conditions, the simulation predicts both better sidewall and bottom coverage in the contact hole than for a conventional sputter deposition process. In Fig. 4, a cross sectional view of one of the contact holes after barrier deposition is shown including both a barrier deposited by CVD (assuming isotropic deposition) and a barrier deposited by collimated sputtering for the conditions described above. It is apparent that the PVD process does not provide a sufficient barrier thickness inside the structure and therefore CVD should be used for barrier deposition.

Step coverage of sputtered metal films better than predicted by simulations has been measured for tantalum layers and can be attributed to re-emission of the metal atoms from the surface [4]. Therefore the use of tantalum may allow PVD of the barrier layer even for geometries as the one discussed in this work. However, for Ti deposition, simulations based on unity sticking coefficient lead to good agreement of simulations with experimental data [5]. Therefore, the profile simulated for the PVD process based on unity sticking coefficient is realistic and CVD is likely to be used for Ti/TiN barrier deposition in future interconnections.

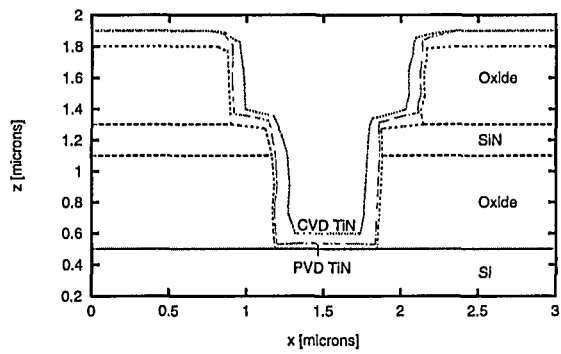

Figure 4: Barrier deposited by CVD in comparison with barrier deposited by collimated sputtering (PVD).

4. Conclusions

We have shown how simulation tools can assist in the development and evaluation of process sequences used in semiconductor manufacturing. In the example we have presented, it turned out as a result of simulations that step coverage of a barrier layer deposited by sputtering, even when using a collimator, is critical. In consequence, it is desirable to use CVD instead of sputtering. In a similar way, by performing etching simulations, different selectivities and anisotropy factors can be evaluated in terms of the geometry of the etched contact holes or trenches. For these simulations however, extensive calibration is necessary to obtain the required simulation parameters.

Acknowledgement

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