A Realistic Methodology for the Worst Case Analysis of VLSI Circuit Performances

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I. Introduction

Minimizing the circuit layout feature size can lead to improved performance, but it may also reduce the manufacturing yield. The smaller dimensions increase the relative variability of the process and make the circuit sensitive to process fluctuations such as, photo mask, depo/etch and furnace. In order to produce circuit designs that are more robust, it is crucial for designers to verify that circuit performances meet specifications across the entire range of process fluctuations. The driving force of previous work has thus been to come up with a simple and effective worst case design[1][2]. In this work, a new approach to statistical worst case of full-chip circuits, using the Principal Component Analysis (PCA) [3] and the Gradient Analysis (GA) [1], is proposed and verified. This method enables designers not only to predict the standard deviations of circuit performance but also to track circuit performances associated with process shift by measuring e-tests. Experimental qualification of the method is described using 0.25μm 256Mega bit DRAM.

II. Methodology and verification

The proposed approach consists of two parts, as shown in Fig. 1. First, we have used a technique incorporating PCA which takes the distributions of SPICE parameters and e-tests as input. Thus each model parameter can be a function of independent e-tests, and a realistic worst case corner can be extracted. Second, the GA is used to predict the standard deviations of circuit performance with a smaller number of model parameters. To verify the approach outlined, the performance parameters of a 256M DRAM were extracted from various positions on wafers. The IV(CV) characteristics are measured, and compact model parameters are finally extracted using the HSPICE level 28 model. We have used pdPCA[4] to determine the minimum number of uncorrelated, independent factors that represent the variability in SPICE model parameters. As shown in Table 1, we find that there are 4-components(factors) which account for 72% of the total variance in process variations. By applying matching algorithms[4], each component can be replaced with Gmmax of 10 μm / 0.56 μm pMOSFET, junction capacitance of n^+p type, sheet resistance of plate-poly and Vth of 3 μm / 25 μm pMOSFET. As a result of PCA, we can construct a typical modeled curve within the measured IV curves of a 10 μm / 0.48 μm nMOSFET, as shown in Fig. 2. From the PCA approach, we can determine the followings:

1) A set of e-tests which can be used to track statistical variations in SPICE model parameters and circuit performance
2) A nonlinear functional relationship between the e-tests and SPICE model parameters

Using 4-components from PCA, with one component at a time skewed to 3σ in the GA approach, the standard deviation σ_P of circuit performance is calculated from

$$\sigma_P = \sqrt{\left(\frac{\partial P}{\partial A}\right)^2 \sigma_A{}^2 + \left(\frac{\partial P}{\partial B}\right)^2 \sigma_B{}^2 + \left(\frac{\partial P}{\partial C}\right)^2 \sigma_C{}^2 + \left(\frac{\partial P}{\partial D}\right)^2 \sigma_D{}^2} \quad (1)$$

where, A, B, C and D are design parameters. In this simple equation, the standard deviations σ_i (i=A,B,C,D) are measured and the gradients, $\frac{\partial P}{\partial i}$ (i=A,B,C,D) are calculated by circuit simulation. In Eq. 1, the GA assumes that circuit performance is a linear function of principal components. This assumption has been verified using circuit simulation for the saturation current Idsat of a 10 μm / 0.48 μm nMOSFET and a 10 μm / 0.56 μm pMOSFET versus 4-component variation, as shown in Fig. 3. As an example of the approach, Fig. 4 compares the variations in the measured 256M DRAM data, namely the read access time, t_{RAC} , with the predicted performance. It is shown that the predicted performance variations agree well with the measured variations. In addition, Fig. 5 shows the t_{RAC} variation versus the 10 μm / 0.56 μm pMOSFET Gmmax variation from PCA and GA. Similarly, junction capacitance of n^+p type, sheet resistance of plate-poly and Vth of 3 μm / 25 μm pMOSFET can be verified, and the sensitivity information can be obtained as shown in Fig. 6. From Fig. 6, we can conclude that 78% of the variation in t_{RAC} is caused by the variation in the 10 μm / 0.56 μm pMOSFET Gmmax. Using above approach, designers are able to calculate realistic performance variations. Moreover, the manufacturing engineers can see how changes in the process are affecting designs.

III. Conclusions

We have applied a combined approach of PCA and GA in order to predict the statistical distributions of circuit performance. As a result, we can determine worst case models before fabrication. Moreover, the approach enables the main effect of circuit performance to be pinpointed, i.e., which process variations influence the circuit performance significantly.

References

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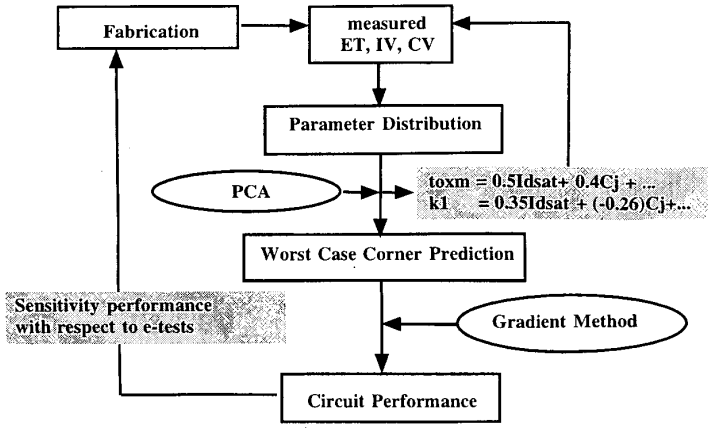

Fig1. Configuration of realistic worst case analysis of VLSI circuits

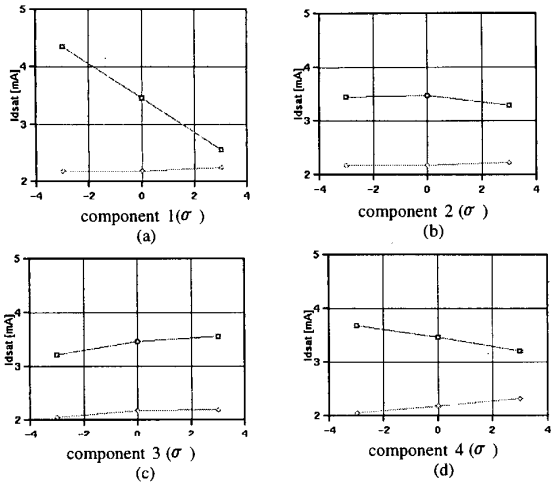

Fig3. Idsat versus variation in Princiapl Component for 10 um / 0.48 um nMOSFET(square) and 10 um / 0.56 um pMOSFET(circle).
(a) Principal Component 1 (Gmmax)
(b) Principal Component 2 (Cj)
(c) Principal Component 3 (Rspp)
(d) Principal Component 4 (Vth)

Table 1. Percentage of the HSPICE level 28 parameter variance which can be monitored by e-tests

	FACTOR1	FACTOR2	FACTOR3	FACTOR4	
Tracking	Gmmax	Cj	Rspp	Vth	SUM [%]
Average	34.0%	15.0%	12.0%	11.0%	72.0%
toxm	90.8%	1.3%	2.2%	0.0%	94.3%
eta0	78.6%	4.8%	1.8%	0.0%	85.2%
k1	43.5%	0.1%	9.6%	0.2%	53.4%
k2	1.6%	3.3%	26.2%	10.1%	41.1%
muz	12.6%	15.1%	4.5%	45.4%	77.6%
phi0	14.3%	30.8%	0.7%	13.7%	59.4%
u00	1.9%	15.1%	12.3%	7.6%	36.9%
u1	0.0%	5.3%	20.4%	25.9%	51.7%
vfb0	45.7%	33.7%	0.1%	0.3%	79.9%
wfac	76.8%	1.1%	1.4%	7.4%	86.6%
x2m	82.6%	0.6%	0.1%	1.2%	84.5%
leta	19.5%	1.9%	40.6%	1.8%	63.9%
lk1	28.8%	11.9%	15.7%	26.5%	82.9%
lk2	7.2%	2.6%	22.9%	44.5%	77.2%
lmuz	5.9%	1.2%	25.0%	51.7%	83.8%
lu0	72.0%	1.1%	12.5%	1.0%	86.7%
lu1	80.4%	0.7%	4.5%	0.7%	86.3%
lvfb	17.0%	30.4%	0.4%	0.1%	47.8%
wk1	13.9%	20.1%	15.1%	13.0%	62.2%

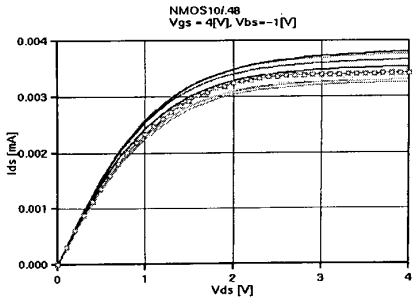

Fig2. IV Characteristics of measured (lines) and calculated(symbol) data

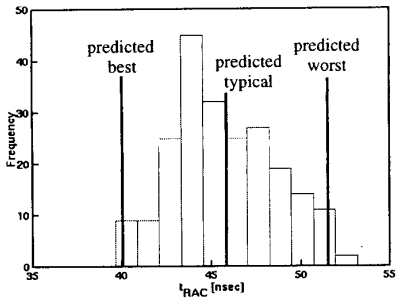

Fig 4. Experimental and simulated read access time, t_{RAC}, from 256M DRAM

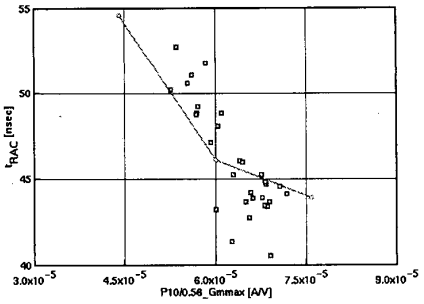

Fig 5. Experimental(symbol) and predicted(line) read access time, t_{RAC}, versus 10 um / 0.56 um pMOSFET Gmmax

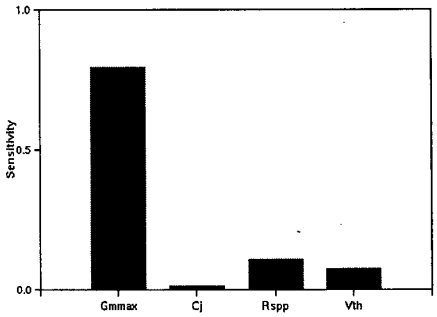

Fig 6. Sensitivity of t_{RAC} with respect to e-tests selected from PCA.