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Accurate Prediction of Hot-Carrier Effects for a Deep Sub-μm CMOS Technology Based on Inverse Modeling and Full Band Monte Carlo Device Simulation

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The ultimate goal of device modeling is the accurate prediction of device characteristics before the technological realization. Due to insufficiencies of process simulation and to a lesser extend of device simulation this goal has not yet been reached [1]. The aim of this work is to reduce the number of wafers in split lots used to investigate the effects of device parameter variation by predicting these effects with device modeling. Our approach is based on a device model (geometry and doping profile) which is extracted for one wafer by inverse modeling (see for example [2]). This model is then used to predict the effects of parameter variation by device simulation with Galene III [3] and our Full Band Monte Carlo (FB-MC) program Falcon [4,5]. In this work we apply the new method to a state of the art 0.25μm-CMOS technology [6] and validate the approach by comparison with experiment.

Our investigation is based on a split lot of wafers which have different channel implants, oxide thickness and source/drain extension implants (Tab. 1). The device geometry and doping profile has been extracted for one of the wafers (No. 9) by inverse modeling. The inverse modeling takes into consideration certain process parameters, measured quantities like the real ploygate length and extensive I-V and C-V data. The doping profile is approximated by 1D and quasi 2D analytical functions which represent the different parts of the profile. This has the advantage that the channel and source/drain extension profiles are directly accessible, making it possible to vary the different profiles independently. In the first step a large area MOS-capacitor is simulated (Fig. 1) and the oxide thickness, polygate doping profile and a rough estimate of the channel profile extracted. The channel profile is then refined by fitting the linear I-V characteristics of a 20μm-transistor for different gate and bulk biases. The source/drain profile is modeled to reproduce the gate-drain capacitance (Fig. 1). In the case of the short channel devices the channel profile is adjusted to account for the reverse short channel effect. Symmetric contact resistances of 4Ω are included. In Fig. 2 cuts through the extracted doping profile for an NMOSFET with 0.22μm polygate length are shown. With this model good agreement between simulation and measurement is obtained not only in the case of linear device behaviour (Figs. 1 and 3) but also in the case of saturation behaviour (Fig. 4) which has been simulated with the generalized hydrodynamic model (GHDM) [3]. The good results found for the saturation current are remarkable, because no fitting has been done in the saturation region. In Fig. 7 the substrate current for wafer No. 9 is shown which has been calculated with FB-MC. The excellent agreement over five orders of magnitude clearly demonstrates that our approach is able to accurately describe hot carrier effects in MOSFETs. Again no fitting has been done to improve the substrate current calculations. The cpu time for one bias point of the substrate current calculation is a few cpu minutes on a Supersparc workstation, demonstrating clearly that FB-MC does not anymore imply prohibitive cpu times.

Based on the device geometry and doping profile extracted for wafer No. 9 we have tried to predict the device behaviour of other wafers without any further fitting. To this end we have assumed that the doping profile in the channel and in the source/drain extensions are proportional to the respective implant dose. In the case of wafer No. 8 we have scaled the source/drain extension profile with a factor of 0.1 due to the ten times smaller implant dose (cf. Tab. 1). In Fig. 5 the drain current within saturation range is shown and reasonable agreement is achieved which is remarkable for such a short channel device, because of the strong dependence of the metallurgical (effective) channel length on the source/drain extension doping profile. Moreover good agreement is found for the substhreshold current which is shown in Fig. 7 together with the substrate current. The excellent results for substrate current show that our approach can also predict hot carrier effects. Furthermore in Fig. 7 results are shown for wafer No. 13 which has a $1nm$ thinner oxide, a higher channel implant and a lower source/drain extension implant dose than wafer No. 9 (cf. Tab. 1). Again good agreement is found for drain and substrate current, validating our approach. Moreover good agreement is found for other wafers not shown here for brevity.

In Fig. 6 the currents of electrons and holes with certain energies hitting the Si/SiO_2-interface of the 0.22μm-NMOSFETs of wafer No. 8 and 9 are shown. The bias conditions are the ones of maximum stress in the allowed bias range ($V_{gate} = 1.5V$ and $V_{drain} = 2.75V$). The shift in the distributions for No. 8 towards the drain (the polygate edge is at $y = 0.11\mu m$) reflects the increase in effective channel length due to the ten times lower source/drain extension implant dose compared to No. 9. The lower peak values of the particle currents due to the field reduction are also caused by the lower doping concentration in the source/drain extensions of No. 8. The decrease is the strongest for the high energetic electrons which are thought to play a crucial rule in the hot carrier degradation process.

Our approach is not only accurate but also very efficient. Since we do not use a process simulation program we can vary parameters of our device model instantly. The cpu times for the solution of the drift diffusion (DD) model and GHDM are about $20s$ and $90s$ per bias point, respectively. This makes rapid evaluation of device characteristics for many different parameter sets possible, which is necessary for the investigation of device parameter fluctuations or device optimization.

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Tab. 1: Oxide thickness (T_{ox}), channel implant dose (I_{chan}) and source/drain extension implant dose ($I_{s/d-ext}$) for the different wafers.

Wafer	T_{ox} [nm]	I_{chan} [cm^{-2}]	$I_{s/d-ext}$ [cm^{-2}]
No. 8	6.3	$6 \cdot 10^{12}$	$3 \cdot 10^{13}$
No. 9	6.3	$6 \cdot 10^{12}$	$3 \cdot 10^{14}$
No. 13	5.3	$7 \cdot 10^{12}$	$3 \cdot 10^{13}$

[1] J. Lorenz (ed.), in *3-Dimensional Process Simulation*, Springer-Verlag, Wien, 1995.

[2] A. Nasr et al., in *Simulation of Semiconductor Devices and Processes* **6**, Springer-Verlag, Wien, p. 126, 1995.

[3] R. Thoma et al., *IEEE Trans. Electron Devices* **ED-38**, p. 1343, 1991.

[4] Chr. Jungemann et al., in *Simulation of Semiconductor Devices and Processes* **6**, Springer-Verlag, Wien, p. 222, 1995.

[5] To be published.

[6] I. Izawa et al., *IEDM Tech. Dig.*, p. 941, 1994.

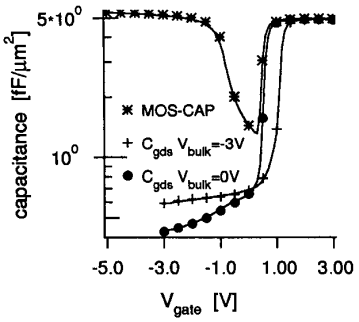


Fig. 1: Capacitance of a large area MOS-capacitor and gate/drain-capacitance for wafer No. 9 (symbols: simulation, lines: experiment).

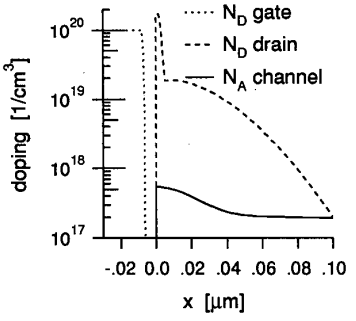


Fig. 2: Doping concentration in the source/drain extensions for $y = 0.11\mu m$ (polygate edge), gate and channel for the $0.22\mu m$-NMOSFET of wafer No. 9.

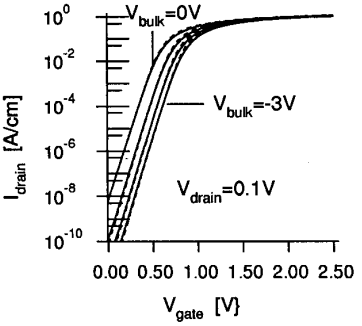


Fig. 3: Drain current in the sub-threshold region for the $0.22\mu m$-NMOSFET of wafer No. 9 (solid lines: experiment, dashed lines: DD-simulation).

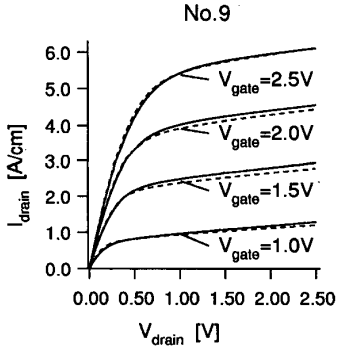


Fig. 4: Drain current in the saturation region for the $0.22\mu m$-NMOSFET of wafer No. 9 (solid lines: experiment, dashed lines: GHDM-simulation).

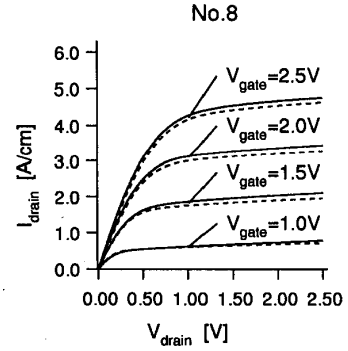


Fig. 5: Drain current in the saturation region for the $0.22\mu m$-NMOSFET of wafer No. 8 (solid lines: experiment, dashed lines: GHDM-simulation).

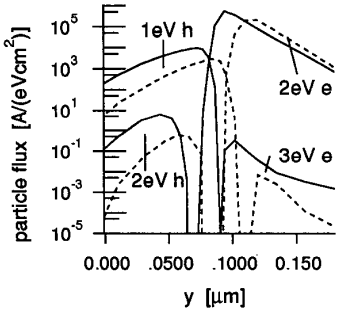
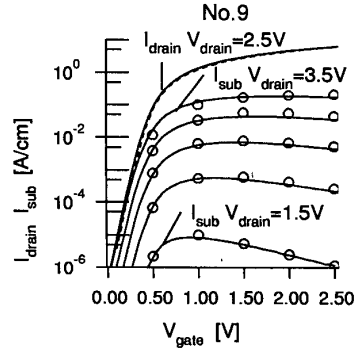
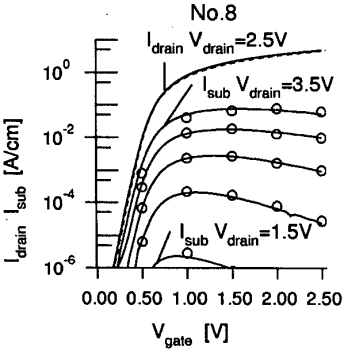


Fig. 6: Currents of electrons and holes with certain energies hitting the Si/SiO_2-interface for the $0.22\mu m$-NMOSFETs of wafer No. 8 (dashed lines) and 9 (solid lines).





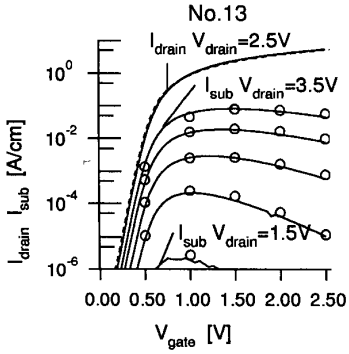


Fig. 7: Drain and substrate current for the 0.22μm-NMOSFETs of the wafers No. 8, 9 and 13 (solid lines: measurement, dashed lines: GHDM, symbols: FB-MC).