Capacitance Model of Microwave InP-Based Double Heterojunction Bipolar Transistors

C. J. Wei, H.-C. Chung, Y. A. Tkachenko and J. C. M. Hwang

19 Memorial Drive West, EECS Department,
Lehigh University, Bethlehem, PA 18015, USA

Abstract

A capacitance model for microwave Double Heterojunction Bipolar Transistors (DHBTs) is presented to account for their special behavior in small-signal S-parameters. A physical picture of barrier effects in DHBTs is described.

1. INTRODUCTION

InP-based double heterojunction bipolar transistors (DHBTs) are attractive for millimeter wave power applications due to their impressive power performance at high frequencies[1]. Output power of 5W/mm at 9 GHz with maximum oscillation frequency of 96 GHz has been reported[1]. The key technique is incorporation of a spacer layer between the broad-band InP sub-collector layer and InGaAs base layer to reduce the barrier which otherwise hinders collection of injected electrons. However, a barrier can not be completely eliminated resulting in a number of effects at both dc and Rf[2].

In this paper we present a capacitance model for DHBTs which accounts for the barrier effects on S-parameters. The model gives an insight into electron accumulation at interface of the barrier. It is found that fitting of the peculiar frequency behavior of the device can not be achieved without an appropriate capacitance model.

2. MODEL

Typical layer structure of the DHBT is shown in Table 1. The collector of the device consists of several layers. A spacer layer of undoped-InGaAs on the collector junction interface and a thin layer of heavily-doped InP thin layer lower the barrier height and move it towards the collector space-charge region of the reversed biased collector-base junction as shown in Figure 1. When electrons flow from the base towards the space-charge region, dynamic electron accumulation, 2D electron gas(2DEG), occurs at the trench of the barrier.

Analogous to the MOS capacitance, a collector-base junction capacitance model in presence of the barrier can be described by a depletion layer capacitance C_d in parallel with a series R_e-C_e elements as shown in Figure 2. The latter represents the 2DEG storage charge with a charging time constant, $\tau_d= R_e C_e$. The time constant τ_d represents the response time of charge build-up under voltage/current variation across the space-charge region. At lower frequency, when the period of signal is longer than τ_d, the 2DEG screens the depletion capacitance. With frequency increasing, however, the depletion capacitance graduately dominates. The difference of this model from a MOS capacitor model is in that the capacitance is both current and voltage controlled whereas the MOS capacitance is solely voltage-controlled. The current dependence originates from the variation of 2DEG density with collector current.

All parameters of the model including the time constant τ_d are dependent on the layer structure, the barrier height and the electric field distribution. Also they are bias-dependent. At lower collector voltage, the collector region is not completely depleted as shown by the simulated electric field profile of Figure 1. The 2DEG causes a step change in the field profile. Note that for a given collector-base voltage. When 2DEG is the only type of space charge, a decrease in 2D-gas density causes a shrink the depletion region resulting in increased C_d. Therefore, the capacitance is expected to be increasing with collector current at higher frequency where C_d dominates. At lower frequency, a variance in the 2DEG can easily follow the current variance and an increasing current gives rise to an increasing capacitance C_e.

3. RESULTS

Bias-dependent S-parameters of a InAlAs-InGaAs-InP DHBT were measured with HP8510 from 0.2 to 30 GHz. The device comprises 12 emitter finger 2 by 10 um. A highly consistent equivalent circuit element extraction method[3] was used to obtain the intrinsic and extrinsic collector impedance values and their frequency dependence. Fig. 3 plots the intrinsic C-B capacitance vs frequency at V_c= 2 V for various injection levels.

At higher voltages, the barrier is diminished by the lowering effect of a higher field. From figure 3, there exists a turning frequency, f_{ct}=1.5 GHz above which the depletion capacitance dominates. The associated time constant is $\tau_d=1/(2\pi f_{ct})=105$ ps. It is also shown that the capacitance increases with collector current below f_{ct} and decreases somewhat for lower current biasing above that turning frequency, as shown in Fig.4. Using fitting technique it is straightforward to obtain the bias-dependent capacitance as well as bias-dependent time constant τ_d.

Incorporating this capacitance model into a small-signal equivalent circuit with LIBRA, a commercial software by EEsof, as shown in Figure 2, the fitting of S-parameters are considerably improved in comparison with conventional model. Fig. 5 shows compares measured S11 and S21 at V_c= 2V and I_b= 1 mA with those obtained using conventional model. A Peculiar kink in S21 makes the accurate fitting very impossible. Fig. 6(a) and 6(b), in contrast, show excellent fitting of measured S-parameters by the modified model. The kink apparently corresponds to the turning frequency f_{ct}. The fitting parameters are listed in Table 2.

4. CONCLUSIONS

For the first time a base-collector capacitance model for DHBTs was constructed to account for the dynamic electron accumulation at InGaAs/InP collector heterojunction. This accumulation gives rise a peculiar frequency dependence of S-parameters, namely a kink in S21, which was accurately predicted by the model. As a results, valuable insight into the dynamics of electron charge build-up is obtained.

Reference

[1] M. Hafizi, P.A. Macdonald, T. Liu, D.B. Rensch and T.C. Cisco, "Microwave Power Performance of InP-based DHBTs for C- and X-band Applications," in *Digest of 1994 IEEE MTT-Symposium*, pp.671-674, San Diego, May 1994

[2] R.A. Sugeng, C.J. Wei, J.C.M. Hwang, J.I. Song, W.P. Hong and J.R. Hayes, "Junction Barrier Effects on the Microwave Power Performance of DHBTs", in *Proc. IEEE/Cornell Conference on Advanced Concepts in High-speed semiconductor Devices and Circuits*, Ithaca, Aug. 2-4, 1993, pp.52-61

[3] C.J. Wei and J.C.M. Hwang,"A new method for direct extraction of HBT equivelent circuit elements" in *IEEE MTT-S Int'l Microwave Symp. Dig.*, 1994, pp.1245-1248

Table 1 Material structure of InP power HBTs.

Name of Layer	Material	Doping(/cm^3)	Thickness(nm)
Cap	n^{++}InGaAs	2x10^{19}	200
Emitter	n^{++}InGaAs	2x10^{19}	230
Emitter	n InAlAs	1x10^{17}	70
Emitter	n InAlAs	1x10^{18}	5
Spacer	i InGaAs	undoped	15
Base	p^{++}InGaAs	2x10^{19}	60
Spacer	i InGaAs	undoped	10
Spacer	n^{++}InGaAs	2x10^{18}	5
Collector	n^{+} InP	2x10^{18}	15
Collector	n InP	5x10^{16}	100
Collector	n InP	1x10^{16}	300
Collector	n^{++}InP	2x10^{19}	100
Sub-collector	n^{++}InGaAs	2x10^{19}	500
Substrate	SI InP	Compensated	5 mil

Table 2 Fitting parameters of equivalent circuit. *Vc*=2 V, Ib=1 mA.

Rb(Ω)	0.75	Cex(pF)	0.239
Lb(nH)	0.051	Cd (pF)	0.41
Re(Ω)	1.56	Re'(Ω)	82
Le(nH)	0.018	C'(pF)	0.85
Rc(Ω)	0.54	Cbe(pF)	3.82
Lc(nH)	0.047	α	0.997
Rb2(Ω)	2.75	Rbe(Ω)	0.31
		τc (ps)	0.13

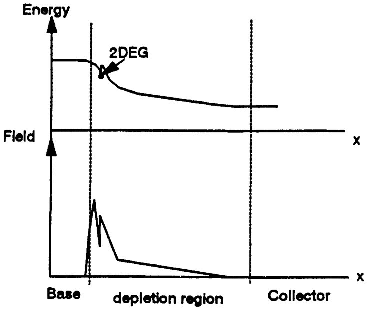


Fig. 1 Band & Field diagram in collector depletion region of DHBTs. The barrier is located in collector depletion region.

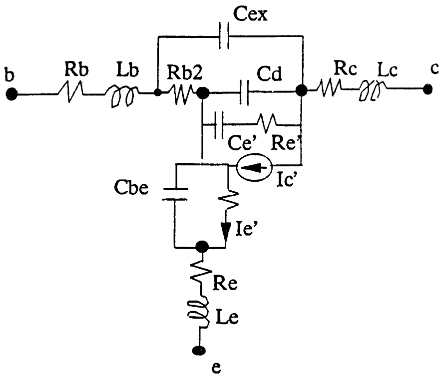


Fig. 2 Equivalent circuit of HBTs. Note the impedance between base and collctor.

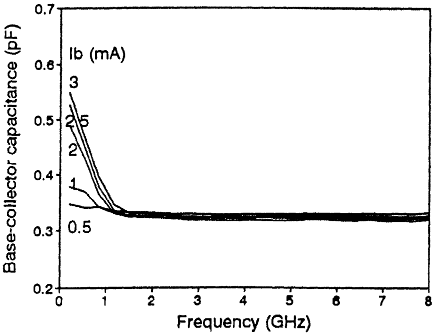


Fig 3 Total base-collactor capacitance as functions of frequency. *Ib* = 0.5, 1, 1.5 and 2 mA.

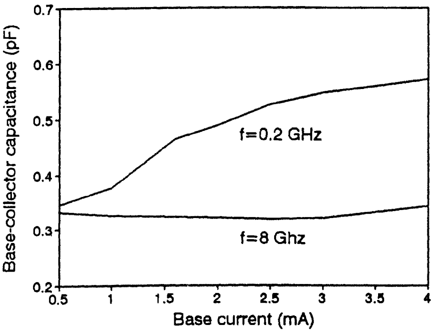


Fig. 4 Total effective Base-colletor capacitance vs. base current for *f*= 0.2 and 8 GHz respectively.

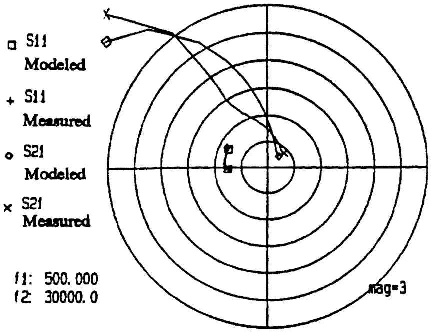
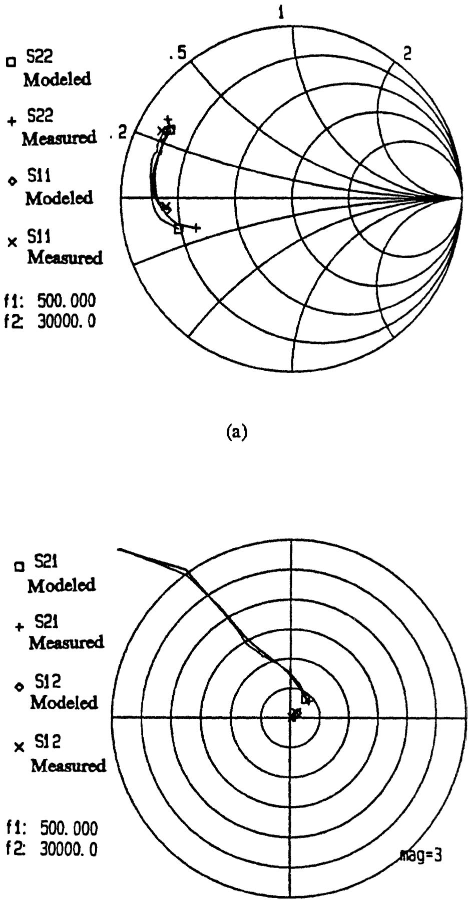


Fig. 5 S-parameter fitting using conventional model.



(a)

(b)

Fig. 6 S-parameter fitting using new model. (a) S11 and S22, (b) S21 and S12