T2CAD: Total Design for Sub-um Process and Device Optimization with Technology-CAD

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Abstract

"T2CAD (Total-Technology-CAD)" is proposed as an application technology of process & device simulators, which provides useful and important data for VLSI process design and optimization. It includes (1) reliability & accuracy of TCAD simulations and (2) process and device optimization method with TCAD, as well as (3) application methodology to VLSI chip design. A sub-um CMOS technology for Mega-bit DRAMs has been optimized based on T2CAD.

1. Introduction

Trends of Dynamic Random Access Memory (DRAM) and MOST feature size in VLSI's are well-known. As for DRAM integration, the bit density has doubled every three-years. To achieve this high integration in VLSI's, process and device feature sizes have been scaled-down to 0.3 um in 1994. On the way toward this sub-half micron process & device technology, many physical phenomena for TCAD application have been highlighted as shown in Fig. 1. All of these critical phenomena required intensive TCAD simulations and careful experimental verifications. However, the use of TCAD in process and device design and optimization for sub-um technology looks less successful because of difficulties in achieving simulation accuracy and experimental verification.

In this paper, a TCAD strategy towards a practical application tool will be discussed for updated VLSI process, device and circuit development [1]. To achieve better prediction with TCAD, a process database for low-temperature impurity diffusion has been constructed [2], incorporating compact modeling of the TED (Transient Enhanced Diffusion) effect. Drain current database has also been developed to calibrate current driving capability of sub-um CMOS devices [3]. Process and device optimization was conducted by the full use of advanced Response Surface Method using the experimental global calibration approach [4,5]. Based on the optimized process and device, circuit model parameters were generated to support a worst case circuit design before fabrication using a test structure.

These basic TCAD technologies were utilized successfully to design a sub-um CMOS process, device and circuit in Mega-bit DRAM development. Experiments show good agreement with predicted device characteristics, and the fabricated DRAM demonstrates good performance and yield.

2. Basic Technology

2.1 Process and Device Database

Process and device databases used in the TCAD calibrations are important to obtain reliable prediction data from TCAD. In the process database, we focused on TED phenomena, which is increasingly important in shallow junction formation with lowered annealing temperature. In the device database, we summarized drain current in sub-um CMOS. It is noted that an anomalous degradation of the CMOS current driving capabilities have been clarified even for the Vdd=3.3V condition. The physical mechanism of the degradation is found to be caused by carrier velocity saturation effects even at the source end of channel.

(A) Process database

Over 300 samples of different implanted dose/energy and annealing temperature/time were fabricated for Phosphorus, Boron, BF2 and Arsenic as dopants. The final depth profiles were measured by SIMS analysis using the CAMECA-ims4f. To parameterize the TED effect, we extracted a compact "TED" parameter of effective diffusivity (D*/Do) based on the experimental doping profile. The TED coefficients for phosphorus is shown in Fig. 2, as functions of implant doses and annealing temperature. It shows that the TED parameter is constant with an error <1.5% when the dose is higher than $1x10^{14}/cm^2$, and no transient enhanced diffusion is observed when the implant dose is under $1x10^{13}/cm^2$. It is noted that the TED parameter is closely independent to implant energy and annealing time.

Experimental samples used in constructing the TED database varied as follows:

- Phos.: Dose (1013-2x1015 cm-2), Energy (30K-3M eV), anneal Temp. (850-1000 C),
- Boron : Dose (5x1012-1016 cm-2), Energy (20K-3M eV), anneal Temp. (900-1000 C),
- BF2 : Dose (2x1013-2x1015 cm-2), Energy (5K-100K eV), anneal Temp. (900-1000 C),
- As : Dose (1.5x1015-3x1015 cm-2), Energy (40K-100K eV), anneal Temp. (850-950 C).

In summary on the TED database, phosphorus implant and diffusion showed the highest TED effect especially at lowered temperature annealing. The TED effect has to be taken into the account for boron implant and diffusion for accurate simulation. Arsenic diffusion is much more complex due to clustering phenomena, which cannot be parameterize with the simple TED model. We are studying further the RTA process for sub-quarter um CMOS process.

(B) Drain current database

One of the vital issues for high-speed VLSI's is current driving ability of component devices. Historically, a simple scaling-down approach has been believed to enhance the MOS device performance as well as to achieve high density VLSI. However, we found an anomalous degradation of sub-um MOS device performance based on a study of intrinsic drain current which eliminates geometrical-effects and two-dimensional field-effects. To characterize this effect, a drain-current database has been developed, and analyzed based on a compact model with carrier velocity saturation. In Fig. 3, the database characterizing the degraded drain current is shown for a NMOS. It clearly exhibits performance loss in shorter channel length when evaluating the normalized (W/L=1) drain current "Idso" at a constant effective gate bias (Ve=Vg-Vt). Note that the degradation occurs even for the device with L=2um at Vdd=3.3V, and lower Vdd cause a less performance loss in shorter channel devices. This data can be used in calibrating device simulation results in terms of the drain characteristics (I-V curves) prediction for sub-um CMOS, which is an essential requirement to provide a reasonable parameter-set for I-V curves with prediction error <3%.

To understand the physical mechanism of the degraded current driving shown in Fig. 3, we newly formulated the effect based on the fact that weak velocity-saturation of carrier

dominates the carrier flow at the source end of channel. The model leads to good agreement with experiments in sub-um NMOS, showing the Ids~$L^{-0.54}$ relation.

2.2 Optimization Technology

A new methodology in simulation-based CMOS process designs has been proposed, using a hierarchical RSM (Response Surface Method) and efficient experimental calibrations. The new design method has been verified in half-um CMOS process/device development, which results in reliable prediction of the threshold voltage (Vth) and drain current (Ids) within 0.01V and 0.84% error, respectively.

The basic idea behind RSM is shown in Fig. 4. In NMOS Vth design, first design-parameters have to be specified, such as gate oxide thickness (Tox) and gate length (Lg) as variables. To obtain systematic data of Vth (Tox, Lg) at specific bias conditions, one can get a Vth data-matrix from nine-point TCAD simulations, just like experimental device measurements of test structures with various fabricated wafers.

The response (Vth) to variables (Tox, Lg) can be approximated with a RSF (response Surface Function) in quadratic form, which can be used in Vth design and optimization.

We fully use the RSM to optimize and design sub-um CMOS process and device. However, in practice, two major drawbacks are found that need to be overcome to give reliable predictions. Since physical models used in process/device simulators are known to be insufficient, even if we use the process database, direct use of RSM based on TCAD simulation may cause significant errors in predicted results of Vth and Ids. To overcome this drawback, we have proposed an efficient calibration method, after the formation of the RSF with minimal number of experimental data. Another drawback is that the design table has to be fixed before conducting a series of RSM design. In practice, one often finds another variable which turns out to be of interest after the completion of a set of simulations. To improve this situation, we have developed a new design strategy, which provides an effective hierarchical design in the above case [6].

Note that in conducting RSM design, (1) pre-conditioning of the variable and response is extremely important to achieve a reliable RSF, which require intensive variable & response transformations to get a linearized relationship between the two, (2) systematic global calibration based on reliable experiments is unavoidable especially for Vth design and analysis, and (3) the range of the variable has to be considered carefully, since the RSF is less reliable if the variable exceeds the range defined in the design table.

Fig. 5 shows an example of the design table and TCAD-responses to Vth and Ids(max). A composite design matrix is used in this case and all the variables and Ids(max) are transformed into a "log(x)" form. After 27-case numerical process and device simulations, a RSF for the Vth is derived, and compared with original simulation results as shown in Fig. 6. As demonstrated in the figure, the RSF coincides with original data within the average error of 0.026V. However, if we compare with experimental data of fabricated devices, significant discrepancy between the RSF and measurement occurred as demonstrated in Fig. 7. It is noted that this discrepancy is not a special case but observed in most cases in sub-um CMOS Vth analysis. It may be caused by insufficient two-dimensional diffusion modeling and unexpected process-condition error. To overcome this problems, a systematic global calibration on the RSF has to be conducted, which results in a good fit between a new RSF and experiments as shown in Fig. 8. The resulting calibrated RSFs for the Vth and Ids is shown in Fig. 9. The error of the new Vth-RSF is less than 0.02V.

Once we get this RSF, efficient process and device design can be done in sensitivity analysis, process optimization and parametric yield prediction, including scaled down device design. An example of process sensitivity analysis on Vth is shown in Fig. 10. Assuming process variation of +/- 10% for Tox, Lg, etc., δTox will cause the largest Vth variation as shown in the figure. However, if one thinks of real control specifications for the process, δVth will be most sensitive to δLg (more than 40% of total Vth variation). Fig. 11 shows Vth analysis based on the RSF. It shows a reasonable Vth-Lg surface for

the variables of Tox, Ncd and Vbb. By using Monte Carlo calculation on the RSF, we can get quite easily predicted distributions of Vth and Ids as shown in Fig. 12. As demonstrated in the figure, the Vth distribution shows a half-Gaussian distribution which reflects a sharp Vth drop in Vth-Lg characteristics. Scaled devices can be also optimized based on the RSF, as shown in Fig. 13. After a 0.65 um NMOS is optimized in terms of Vth=0.35V and Vth-Lg curve, one can optimize a scaled 0.55 um NMOS with the same Vth specification as shown in the figure. Expected Ids increase with the scaled device is 10% in this case.

As demonstrated above, various process and device optimizations have been achieved based on the experimentally calibrated RSF, which gives us many good design choices as well as better quality in process and device optimization in sub-micron CMOS technology.

3. Generation of CKT model parameters

To achieve concurrent design of the process and circuit, precise prediction of circuit model parameters is one of the essential issues in VLSI memory development. Circuit model parameters, such as MOST model parameters, junction and interconnect capacitance, have to be accurately obtained without test chip fabrications. We have developed a practical T²CAD focused on the new global experimental calibrations, which generates process recipe and device performance as well as complete model parameters in circuit simulation for sub-um VLSI memories. A couple of tens of parallel TCAD simulation were conducted based on the RSM statistical design table with optimum variable transformation. The resulting RSF for the objective design parameters (Vth, Ids, BV, etc.) were generated. RSF-design on process and device characterization were performed extensively using sensitivity analysis techniques, parametric yield estimation and global optimization, as mentioned previously. Finally, optimized process and devices were analyzed in detail to generate I-V (C-V) data for a parameter extraction system for circuit simulators.

Fig. 14 shows an example of generated MOS model parameters for a 0.5 um CMOS DRAM. Model fitting error against original (simulated and calibrated) I-V data is 0.85%. Experimental verification of worst case simulation on the predicted Vth-Lg and Ids-Lg characteristics shows reasonable accuracy as shown in Fig. 15. As shown in the figure, fabricated devices shows good agreement with prediction based on the T²CAD within the errors of process-fluctuation limits for the Vth and Ids. The T²CAD used 200hrs CPU on the HP/9000, and took one month in design.

References

[1] H. Masuda et al.; 'TCAD strategy for predictive VLSI memory development', Technical Digest of IEDM'94, pp. 153-156, Dec. 1994.

[2] H. Sato, K. Tsuneno and H. Masuda; 'Evaluation of two-dimensional transient enhanced diffusion of Phosphorous during shallow junction formation,' IEICE Trans. Electron., Vol. E-77-C, No. 2, pp. 106-111, Feb. 1994.

[3] K. Tsuneno, H. Sato and H. Masuda; 'Modeling and simulation of anomalous degradation of submicron NMOS's current-driving due to velocity-saturation effect,' IEICE Trans. Electron., Vol. E-77-C, No. 2, pp. 161-165, Feb. 1994.

[4] G. E. P. Box and N. R. Draper; 'Empirical model building and response surface, John Wiley and Sons, 1987.

[5] H. Masuda, F. Otsuka, Y. Aoki, and S. Satoh, S. Shimada ; 'Response surface method for submicron MOSFETs characterization with variable transformation technology,' IEICE Trans., E-74, Vol. 6, pp.1621-1633, June 1991.

[6] H. Sato et al.; 'A new hierarchical RSM for TCAD-based device design to predict CMOS development', Technical Digest of ICMTS'95, pp. 299-302, March 1995.

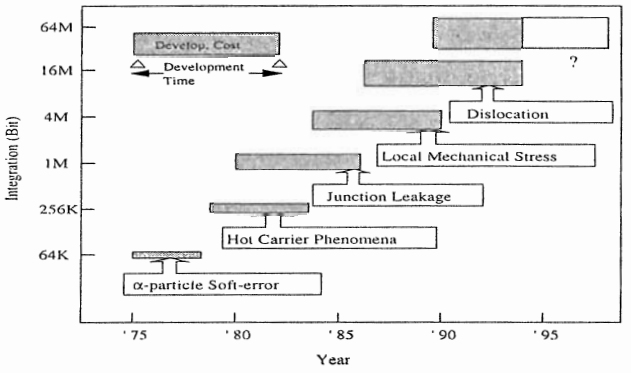

Fig. 1 DRAM trends and TCAD applications.

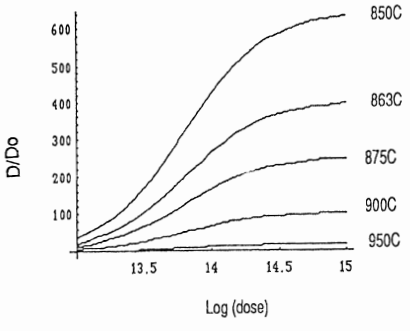

Fig. 2 TED database for Phosphorus.

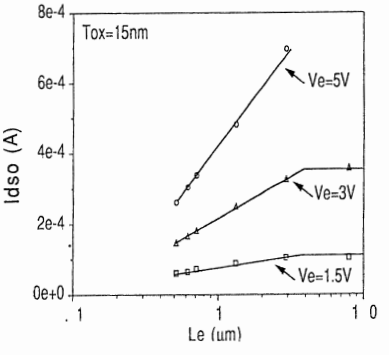

Fig. 3 Drain current degradation in NMOS.

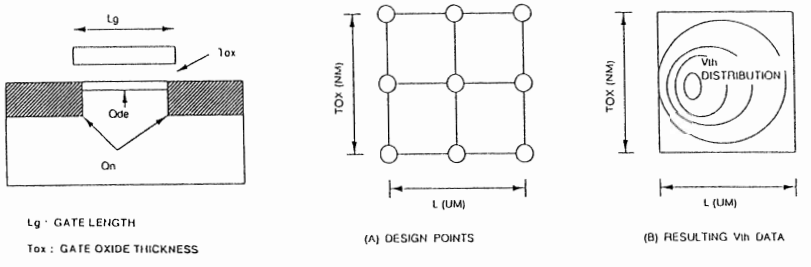

Fig. 4 Basic idea of RSM.

	X1	X2	X3	X4	Lg(um)	Tox(nm)	Qde (/cm2)	Qn- (/cm2)	Ids(5V) (mA)	Vth(V)
1	1.000	1.000	1.000	1.000	1.450	19.570	2.42e+12	1.21e+13	2.487	1.525
2	1.000	1.000	1.000	-1.000	1.450	19.570	2.42e+12	8.30e+12	2.405	1.535
3	1.000	1.000	-1.000	1.000	1.450	19.570	1.65e+12	1.21e+13	3.072	1.202
4	1.000	1.000	-1.000	-1.000	1.450	19.570	1.65e+12	8.30e+12	3.003	1.208
5	1.000	-1.000	1.000	1.000	1.450	13.370	2.42e+12	1.21e+13	4.286	0.930
6	1.000	-1.000	1.000	-1.000	1.450	13.370	2.42e+12	8.30e+12	4.098	0.825
7	1.000	-1.000	-1.000	1.000	1.450	13.370	1.65e+12	1.21e+13	4.968	0.704
8	1.000	-1.000	-1.000	-1.000	1.450	13.370	1.65e+12	8.30e+12	4.790	0.707
9	-1.000	1.000	1.000	1.000	0.990	19.570	2.42e+12	1.21e+13	3.167	1.436
10	-1.000	1.000	1.000	-1.000	0.990	19.570	2.42e+12	8.30e+12	2.589	1.450
11	-1.000	1.000	-1.000	1.000	0.990	19.570	1.65e+12	1.21e+13	3.788	1.090
12	-1.000	1.000	-1.000	-1.000	0.990	19.570	1.65e+12	8.30e+12	3.536	1.108
13	-1.000	-1.000	1.000	1.000	0.990	13.370	2.42e+12	1.21e+13	5.070	0.857
14	-1.000	-1.000	1.000	-1.000	0.990	13.370	2.42e+12	8.30e+12	4.371	0.870
15	-1.000	-1.000	-1.000	1.000	0.990	13.370	1.65e+12	1.21e+13	5.820	0.620
16	-1.000	-1.000	-1.000	-1.000	0.990	13.370	1.65e+12	8.30e+12	5.208	0.633
17	2.000	0.000	0.000	0.000	1.750	16.200	2.00e+12	1.00e+13	3.203	1.099
18	-2.000	0.000	0.000	0.000	0.820	16.200	2.00e+12	1.00e+13	4.668	0.879
19	0.000	2.000	0.000	0.000	1.200	23.600	2.00e+12	1.00e+13	2.265	1.680
20	0.000	-2.000	0.000	0.000	1.200	11.070	2.00e+12	1.00e+13	5.756	0.480
21	0.000	0.000	2.000	0.000	1.200	16.200	2.92e+12	1.00e+13	3.200	1.335
22	0.000	0.000	-2.000	0.000	1.200	16.200	1.37e+12	1.00e+13	4.460	0.795
23	0.000	0.000	0.000	2.000	1.200	16.200	2.00e+12	1.46e+13	4.089	1.025
24	0.000	0.000	0.000	-2.000	1.200	16.200	2.00e+12	6.80e+12	3.633	1.036
25	0.000	0.000	0.000	0.000	1.200	16.200	2.00e+12	1.00e+13	3.870	1.032

Fig. 5 Composite-Design table example.

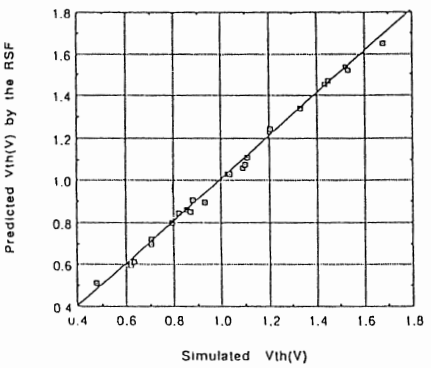

Fig. 6 RSF obtained by a series of TCAD.

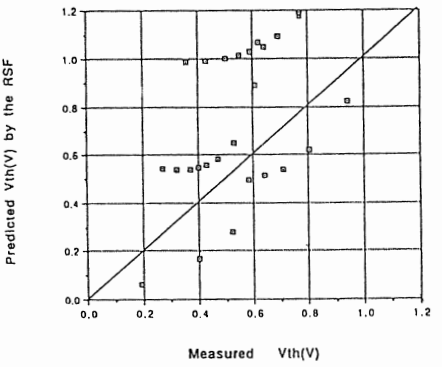

Fig. 7 Experimental error of original RSF.

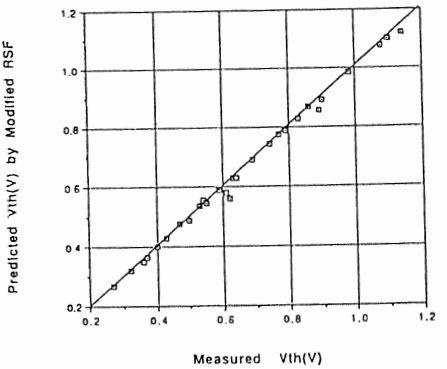

Fig. 8 Experimental verification of calibrated RSF.

$$Vth(V) = 0.59+0.955x_1+0.1057x_2+0.1348x_3+0.0003x_4-0.0080x_1^2+0.00167x_2^2 +0.050x_3^2+0.000062x_4^2+0.0105x_1x_2-0.0237x_1x_3+0.018x_1x_4+0.0121x_2x_3 -0.004x_2x_4+0.003x_3x_4+\varepsilon$$

$$\ln(Ids.max(mA)) = 0.4832-0.0473x_1-0.0636x_2-0.0399x_3+0.0163x_4-0.0002x_1^2 -0.0029x_2^2-0.026x_3^2-0.0004x_4^2-0.0048x_1x_2+0.0024x_1x_3-0.0146x_1x_4 -0.0051x_2x_3-0.0002x_2x_4+0.051x_3x_4+\varepsilon$$

Fig. 9 Obtained RSFs for Vth and Ids.

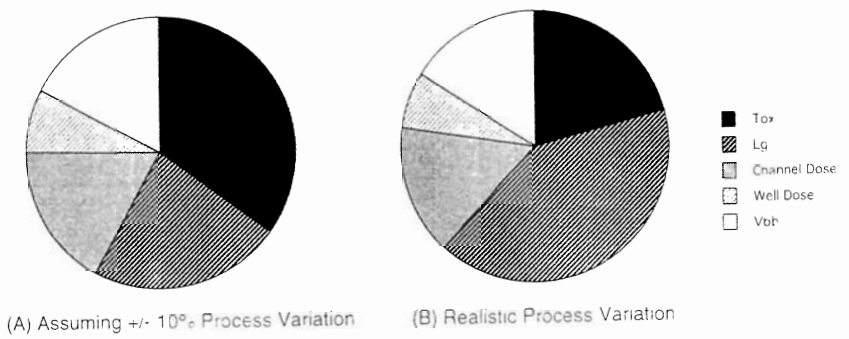

Fig. 10 Process sensitivity analysis of 0.5um NMOS. Region size denotes degree of sensitivity.

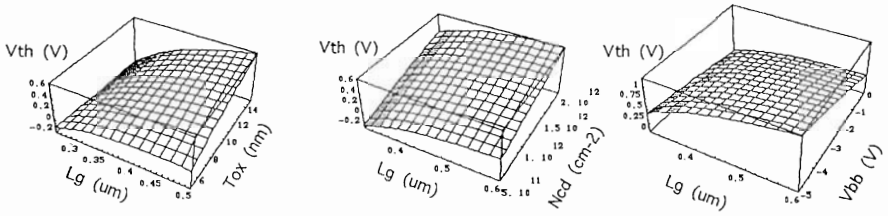

Fig. 11 Predicted Vth-Lg surface based on new RSF.

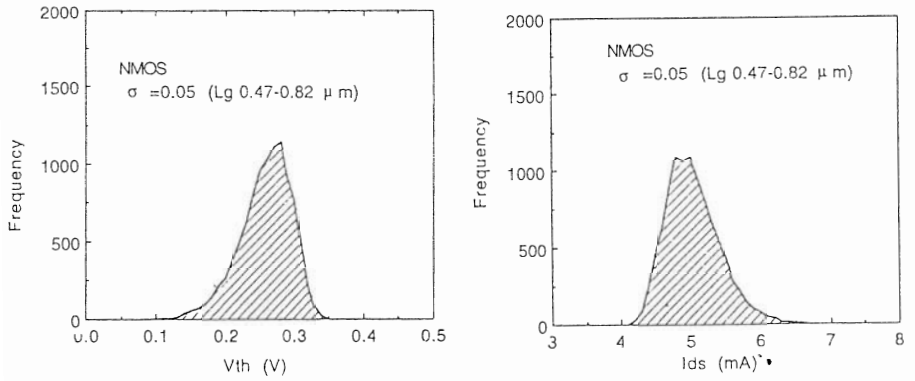

Fig. 12 Monte Carlo calculation on Vth and Ids distributions.

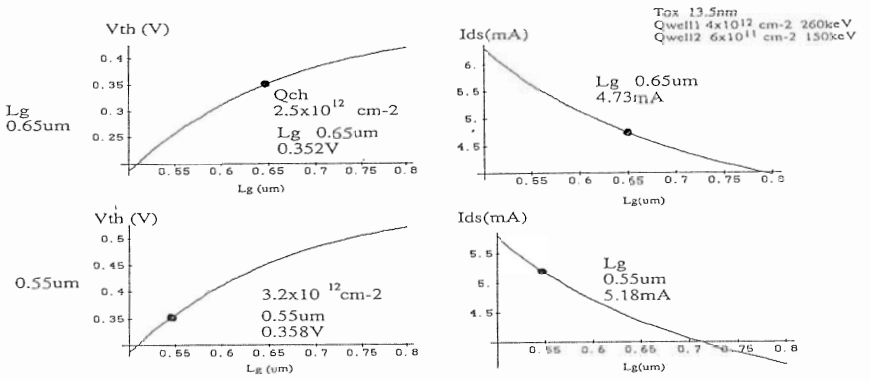

Fig. 13 Example of Vth and Ids design for a scaled device.

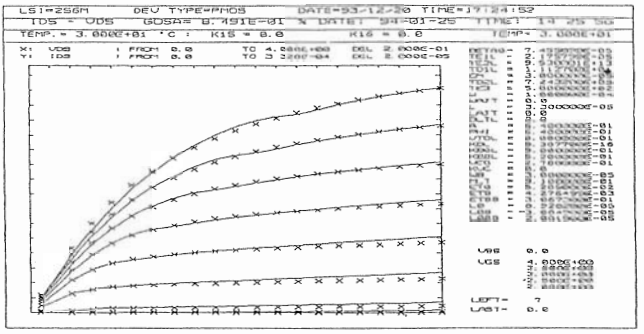

Fig. 14 Generated MOS model parameters based on drain current simulated by the T²CAD.

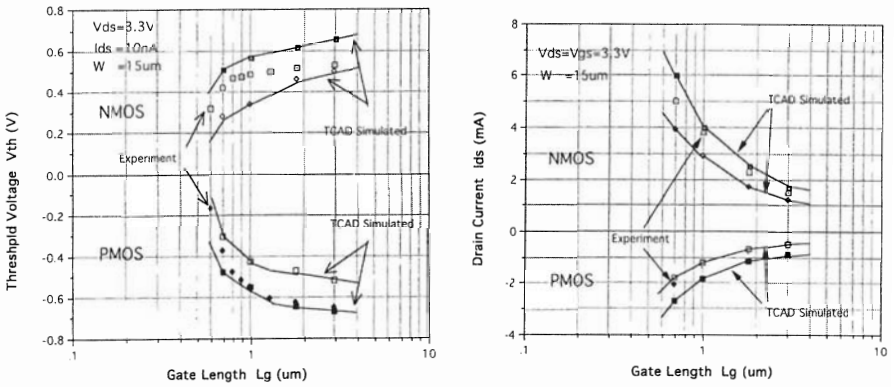

Fig. 15 Experimental verification of generated worst-case circuit parameters. The two TCAD simulations indicate the upper and lower boundary of the worst case parameters