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Simulations of Carrier-Blocking Effects on Cutoff Frequency Characteristics for AlGaAs/GaAs HBTs with Insulating and Semi-Insulating External Collectors

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Abstract

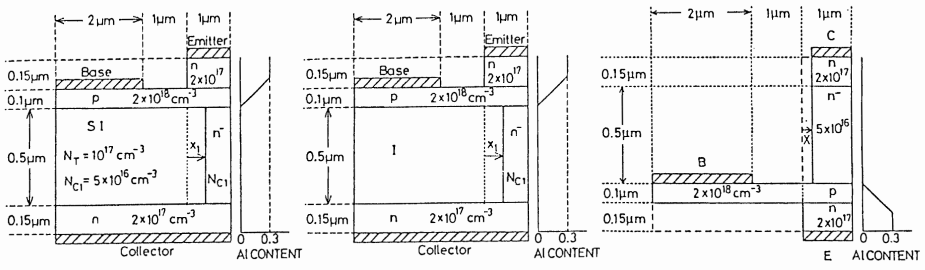
Two-dimensional simulation of AlGaAs/GaAs HBTs with a perfectly insulating external collector is performed. It is shown that the cutoff frequency can degrade heavily due to its carrier blocking effect that leads to an increase in base delay time. In relation to this effect, a design criterion for collector-up HBTs will also be discussed.

1. Introduction

Recently, AlGaAs/GaAs heterojunction bipolar transistors (HBTs) have received great interest for application to high-speed and high-frequency devices. To reduce the parasitic base-collector capacitance and to improve the high- frequency performance, semi-insulating external collectors are often introduced [1]. Also, collector-up HBTs without external collectors are fabricated and examined [2]. In a previous work, we simulated AlGaAs/GaAs HBTs with a semi-insulating external collector [3], and found that the cutoff frequency f_T could degrade when electrons become injected into the semi-insulating layer [4]. In this work, we have simulated AlGaAs/GaAs HBTs with a perfectly insulating external collector and studied how its current blocking affects f_T characteristics. In relation to this, a collector-up HBT is also simulated, and a design criterion for it will be discussed.

2. Physical model

Device structure simulated in this study are shown in Figure 1. (a) and (b) are emitter-up HBTs with semi-insulating (SI) and perfectly insulating (I) external collectors, respectively. We assume that the SI-layer is achieved by introducing a deep acceptor into the n^--layer [3]. (Its density N_T must be higher than the n^--layer doping density N_{C1}.) In the I-layer, current flow is prohibited. Figure 1(c) is a collector-up structure where the external emitter is assumed to be ideally insulating. The Poisson's equation and continuity equations for electrons and holes are solved numerically in two dimension. Here, we concentrate our attention on how the f_T characteristics are affected by the collector structures.



(a) (b) (c)

Figure 1: Device structures simulated here. (a) and (b) are usual emitter-up HBTs with semi-insulating (SI) and ideally insulating (I) external collectors, respectively. (c) is a collector-up HBT with an ideally insulating external emitter.

3. f_T for emitter-up HBTs and carrier-blocking effect

Figure 2 shows f_T versus collector current density I_C curves of emitter-up HBTs with different x_1 in Figures 1(a) and (b). Positive x_1 means that the SI- or I-layer extends into the intrinsic collector region, while negative x_1 means that it is away from the intrinsic collector region. $N_T = 0$ in Figure 2 corresponds to a case with an n^- external collector. It is seen that by introducing a SI- or I-layer, f_T is improved, as expected, when $x_1 < 0$. But, when $x_1 \geq 0$, f_T is degraded and the degradation is much more remarkable for a case with an I-layer. The latter point is an unexpected result. It is understood that when $x_1 > 0$, effective channel width becomes narrow in the collector region and so a high injection condition appears earlier, leading to a lower f_T. However, this situation is similar for the two cases with SI- and I-layers. So, another mechanism for degrading f_T should exist for the case with an I-layer.

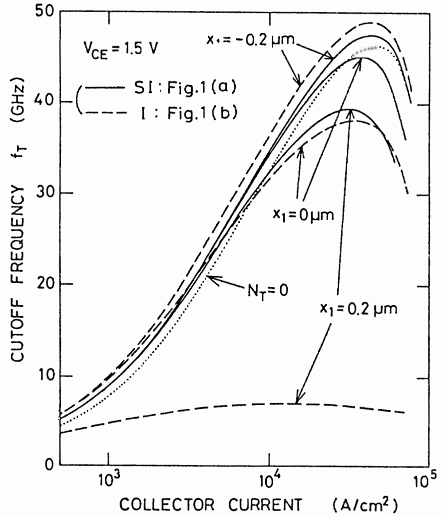
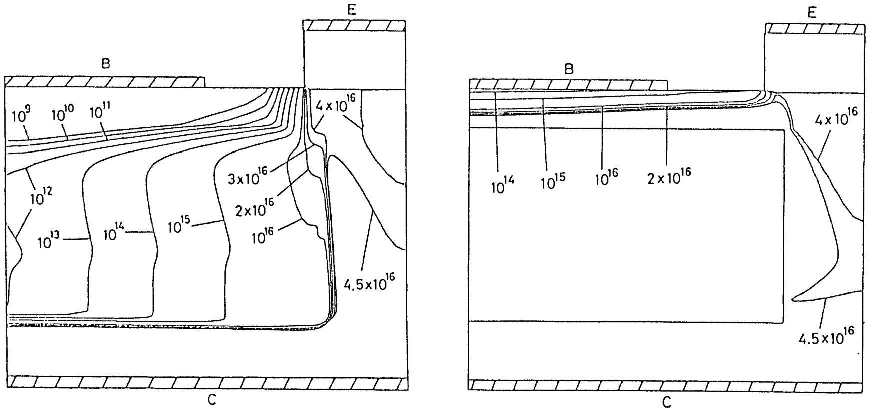


Figure 2: Cutoff frequency f_T versus collector current density I_C curves of emitter-up HBTs, with x_1 as a parameter. $N_T = 0$ corresponds to a case with a usual n^- external collector.



(a) x_1 = 0.2 µm (SI) (b) x_1 = 0.2 µm (I)

Figure 3: Electron density profiles of emitter-up HBTs with different external collectors $V_{CE} = 1.5$ V and $I_C = 6.5 \times 10^4$ A/cm^2.

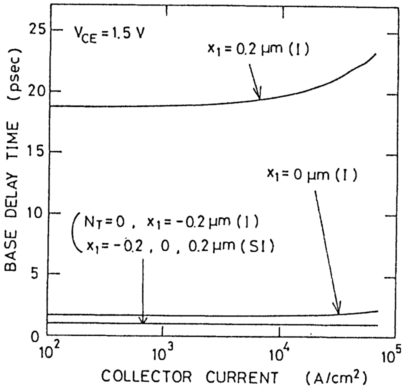


Figure 4: Base delay time versus I_C curves of emitter-up HBTs with different collector structures, corresponding to Figure 2. No remarkable differences are seen for three cases with semi-insulating (SI) external collectors.

Figure 3 shows electron density profiles in a high current region. It is seen that for the case with an I-layer, relatively high densities of electrons exist in the external base region. It is interpreted that these electrons are blocked by the I-layer. In this case, the effective base delay time τ_B becomes very long as shown in Figure 4, because τ_B is given by $(\delta Q_{nB}/\delta I_C)_{V_{CE}}$ where Q_{nB} is electron charges in the base region. Therefore, the remarkable degradation of f_T for the case with an I-layer ($x_1 > 0$) is due to the increase in the base delay time.

4. f_T for collector-up HBTs

The above carrier-blocking phenomenon may become a problem in a collector-up HBT. Figure 5 shows $f_T - I_C$ curves of collector-up HBTs as a parameter of x in Figure 1(c). When $x > 0$, that is, when the collector width becomes narrower than the emitter width,

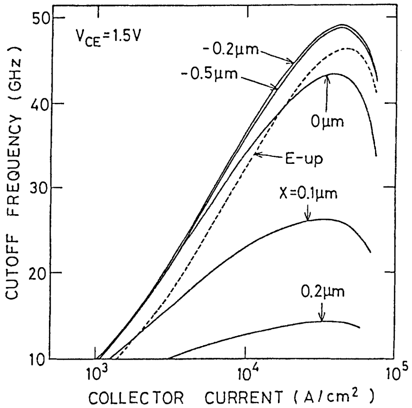


Figure 5: f_T versus I_C curves of colletor-up HBTs (Figure 1(c)), with x as a parameter. E-up corresponds to a case of $N_T = 0$ in Figure 2.

f_T is degraded heavily. This is because, as described before, high densities of electrons are blocked and remain in the external base, leading to a long base delay time. In real devices, the external emitter region is made semi-insulating by proton or oxygen ion-implantation [2]. So, to avoid the above phenomenon, the width of intrinsic emitter region determined by the ion-implantation should be narrower than the collector width.

5. Conclusion

We have shown theoretically that the introduction of a perfectly insulating external collector in emitter-up HBTs may lead to unexpected degradation of f_T due to its carrier-blocking and the resulting increased base delay time. To avoid this phenomenon, the insulating layer should be slightly away from the intrinsic collector region. This means that in collector-up HBTs, the width of effective intrinsic emitter region must be made narrower than the collector width.

References

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