Impact of Cell Geometries and Electrothermal Effects on IGBT Latch-Up in 2D-Simulation

H. Brunner, Y. C. Gerstenmaier, and H.-J. Mattausch

Corporate Research and Development, Siemens AG Otto-Hahn-Ring 6, D-81739 München, GERMANY

Abstract

The influence of the emitter cell geometry of an insulated gate bipolar transistor (IGBT) on the forward behaviour is investigated by electrothermal device simulation. For comparison isothermal device simulation is used at different temperatures. The latch-up behaviour of cellular cell and stripe designs is calculated. As a result the stripe design possesses a higher latch-up ruggedness. However the impact of the cell geometry on IGBT latch-up is affected by electrothermal effects. The variation of the collector-emitter current with the lattice temperature distribution at latch-up is different for stripe and cell designs. The temperature dependence of the junction voltage and the hole current proportion to the total current are electrothermal effects which influence IGBT latch-up.

1. Introduction

The IGBT shown in Fig. 1 is a conductivity modulated MOSFET with a p doped emitter region. The conductivity modulation occures due to the injection of minority carriers into the n⁻ drift region. This device can be operated at high current densities even when designed to support high blocking voltages. However, the IGBT possesses a parasitic four-layer thyristor structure (n^+ source-p base- n^- base-p drain). When the parasitic thyristor is turned on, the collector current cannot be controlled further by the insulated gate and the device is often damaged. This mode is called IGBT latchup. When the hole current which flows underneath the n⁺ emitter region produces a forward voltage drop which exceeds the n⁺ source to p base junction voltage, electrons are injected from the n⁺ emitter into the p base region and turn on the parasitic thyristor. The investigation of IGBT latch-up is an electrothermal problem, due to the temperature dependence of the junction voltage, and other physical parameters. It has been measured, that the latching current decreases with increasing temperature [1]. The simulated structure in Fig. 1 possesses a n⁻ base designed for a blocking capability of 600V. The thermal boundary condition in the case of nonisothermal simulation is represented by a thermal resistance to a heat sink held at 300K which is fixed to the drain electrode. The case of a stripe cell versus a circular cell design with rotational symmetry is considered. A plane view of the emitter geometries is depicted in Fig. 2, the shaded area indicates the minority-carrier collector area which is surrounded by the n⁺ source.

For the numerical investigation of the latch-up behaviour with self heating effects electrothermal simulation is essential [2]. The device simulator MEDICI [3] is used which includes a fully coupled simultaneous solution of Poisson's, carrier continuity

and heat flow equations . For steady state solutions the heat flow equation takes the form $% \left({{{\left[{{{\rm{s}}_{\rm{e}}} \right]}}} \right)$

$$H = -\nabla(\lambda(T)\nabla T) \tag{1}$$

where H is the heat generation determined by the total current density, electric field and the recombination rate. λ is the thermal conductivity of the material. The electron and hole current densities

$$\mathbf{J_n} = qn\mu_n \mathbf{E} + qD_n \nabla n + q\frac{D_n}{T} n\nabla T$$
⁽²⁾

$$\mathbf{J}_{\mathbf{p}} = qp\mu_{p}\mathbf{E} - qD_{p}\nabla p - q\frac{D_{p}}{T}p\nabla T$$
(3)

include an additional current component with the temperature gradient as a driving force. Isothermal simulation is performed by solving the electrical semiconductor equations at constant temperature.

2. Results and Discussion

The n-channel inversion layer in the p base underneath the gate oxide which makes forward conduction possible, is supported by a gate voltage of 20V. The typical IGBT forward characteristics is the exponential rising of the collector-emitter current J_{CE} in the low voltage region and the MOSFET-like current saturation or the latch-up. Static IGBT forward characteristics performed with electrothermal simulation are illustrated in Fig. 3. In the case of the circular cell latch-up occures at $V_{CE}=7.3V$ and $J_{CE}=1148 \text{A/cm}^2$ and the maximal lattice temperature amounts to 377K in the inversion layer of the p base region. For the stripe cell latch-up arises at a higer voltage and current density ($V_{CE}=10.1V$ and $J_{CE}=1360A/cm^2$) with a maximal lattice temperature of 445K . Due to the smaller minority-carrier collector area of the circular cell (see Fig. 2) hole current crowding occures and increases the lateral voltage drop of the hole current beneath the n⁺ source. The stripe cell structure has much less current crowding due to the larger minority-carrier collector area so that the necessary voltage drop for IGBT latch-up arises at a larger collector-emitter current. In Fig. 6 the hole current flow lines, the electron concentration and the internal lattice temperature distributions in the device are shown at the bias point A of the stripe cell. The electron concentration indicates the beginning of electron injection into the p base, which initiates the turn on of the parasitic thyristor. The results of isothermal simulation at the constant lattice temperatures 300K and 400K are shown in Fig. 4-5. At 300K the collector-emitter voltage of the circular cell amounts to 80V when latchup occures and the stripe cell represents at this temperature a latch-up safe device until the blocking voltage is reached. At temperature of 400K (Fig. 5) the circular cell latches at V_{CE} =13.1V and J_{CE} =1516A/cm² the stripe cell at V_{CE} =315V. The built-in voltage of the n^+ source p-well junction decreases with temperature and is the dominating thermal effect in the isothermal calculations. Considering the circular cell, in the non-isothermal case with $T_{max}=377$ K latch-up occures at a lower collectoremitter current compared to the isothermal case with T_{max} =400K. In this comparison the variation of the hole current proportion with non-isothermal conditions plays an important role. The cross sections of hole currents (Fig. 7) and temperature distributions (Fig. 8) at constant collector-emitter current show the relationship of these physical quantities for different thermal conditions. The difference of the hole currents at the isothermal temperature distributions 300K and 400K are relatively small. The highest hole current occures (solid line) at non-isothermal temperature distribution





Figure 6: hole current flow lines, electron concentration, temperatur contours $(T_{max}=445K, \Delta T=5K)$ for stripe design at bias point A (darker color \rightarrow higher value)



Figure 7: cross sections of hole currents at $J_{CE}=1000A/cm^2$ for circular cell at x-x axis



Figure 8: cross sections of temperatures at $J_{\rm CE}{=}1000A/{\rm cm}^2 ~{\rm for~circular~cell~at~x{-}x~axis}$

in the IGBT. The quasi-isothermal case is computed with a very large thermal conductivity, chosen as $\lambda = 10^5 \lambda_{Si}$ ($\lambda_{Si} = 1.4 \text{ W/cmK}$). Hence, the temperature gradient tends to zero and the gap between the non-isothermal and isothermal hole current distributions becomes small. This example shows that the temperature gradient in the device which holds the n-channel and the p-emitter at different temperatures influences the hole current proportion and therefore the latch-up sensibility. Thus the IGBT latch-up properties which occures in the non-isothermal investigation cannot be explained by the absolute temperature near the n⁺ source area only.

3. Conclusion

The impact of cell geometries on IGBT latch-up are shown for circular and stripe cell designs by electrothermal simulation. In the case of the circular cell current crowding reduces the latch up current. However the magnitude of this cell geometry effect is clearly influenced by temperature. The difference between the latch-up currents varies with the temperature. The temperature dependence of the junction voltage is the dominating effect at isothermal conditions. In the non-isothermal case the variation of the hole current proportion with temperature gradient plays an important role for IGBT latch-up. The temperature gradient term of Eq. (2) and (3) cannot explain this increased hole current proportion in the non-isothermal case, because its contribution is to small and of opposite sign. This question is still unsettled, therefore further investigations are necessary.

References

- B.J.Baliga, "Temperature behavior of insulated gate transistor characteristics," Solid State Electron., 28, pp.289-297 (1985)
- [2] V. Axelrad, R.Klein "Electrothermal Simulation of an IGBT" Proceedings of 1992 ISPSD, Tokyo, pp.158-159
- [3] Technology Modeling Associates, Inc., Palo Alto, California, USA. MEDICI users's manual, Jan 1992.