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Study of 3-D Effects in BOX Isolation Technologies

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Abstract

This paper reports on three-dimensional simulation of box isolation technologies in order to quantify the leakage currents due to the contribution of the lateral and vertical parasitic MOSFETs formed in conjunction with trench isolation. A new mode of leakage current caused by intrinsic 3-D effects is described which may pose serious problems for future scaling of the minimum n^+ to p^+ spacing.

1 Introduction

Trench isolation was originally proposed for use in bipolar technologies but has recently received increased attention as an attractive alternative to LOCOS or LOCOS-like isolation schemes in CMOS processes, because it offers a 2-5X reduction in the minimum device separation when compared with LOCOS-based isolation techniques [1]. Despite the higher integration capability, trench isolation in MOS technologies presents a number of problems associated with the fabrication of deep trenches as well as problems arising from the electrical properties of the parasitic MOSFETs formed in conjunction with the trenches. This paper addresses the latter problem.

Fig. 1 shows the lateral and vertical parasitic NMOSFETs formed in a p-well surrounded by an oxide trench, where the trench oxide acts as the gate insulator of the parasitic MOSFETs. Under typical bias conditions, substantial leakage current can result due to inversion along the trench sidewall. In an earlier work, Cham *et al.* [2] attributed this leakage current mainly to inversion of the vertical channel along the trench sidewall by fixed charge in the oxide-filled trench, where the problem of inversion along the trench surface was studied in terms of the vertical parasitic MOSFET using two-dimensional simulation. The standard techniques used to reduce the leakage current, which include 1) offsetting the source/drain from the trench isolation, and 2) trench sidewall implantation, tend to increase process complexity and/or the minimum n^+ to p^+ spacing. More recently, Kasai *et al.* [3] achieved 0.25-μm well-to-well separation using a deep boron implant in the p-well to form an effective sidewall channel stop, raising the threshold voltage of the vertical parasitic MOSFET to 15V, and, thus, suppressing large leakage currents along the vertical channel. However, future scaling of the n^+ to p^+ spacing, limited by the leakage current of the lateral parasitic MOSFETs, has yet to be fully characterized.

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This paper analyzes both the lateral and vertical parasitic MOSFETs formed in conjunction with the conventional MOSFET on the silicon mesa. In this work, the 3-D device simulator SECOND [4] was used to quantify the contribution of the parasitic MOSFETs as a function of channel and well doping, trench width, and bias conditions. The I-V characteristics as a function of technology parameters for the conventional MOSFET, including parasitics, along with derivation of design rules for box isolation technologies has been described in [5]. In this paper, the emphasis is placed on describing a new mode of leakage current caused by intrinsic 3-D effects.

2 Three-Dimensional "Corner" Effect

A cursory look would suggest the effects of the parasitic MOSFETs can be quantified using two-dimensional simulation by separately evaluating the conventional and parasitic MOSFETs and summing the currents appropriately. However, as illustrated in Fig. 2, the electric field lines stemming from the conventional and parasitic gate become concentrated in the corner region where the gate and trench oxide adjoin. In subthreshold, the crowding of the electric field lines leads to formation of a one-dimensional inversion channel along the edge of the conventional channel. A purely 2-D approach would fail to predict the onset of drain current due to the presence of this cooperative, three-dimensional "corner" effect. This is illustrated in Fig. 3, where curves 1 and 2 represent, qualitatively, the I_D-V_G behavior for the conventional and parasitic MOSFETs, respectively, excluding any interactions. The 3-D effect, as shown, is the difference between the full simulation including all interactions and the sum of curves 1 and 2, which is what would be predicted by a purely 2-D approach.

To illustrate the extent of the 3-D effect, the current modes as a function of gate voltage V_G and parasitic gate voltage V_{PG} are summarized in Fig. 4, where V_T and V_{PT} represent the threshold voltage of the conventional and parasitic MOSFETs, respectively, calculated assuming no 3-D effects. In subthreshold, the gate biases for both the conventional and parasitic MOSFETs are sufficiently lower than the corresponding threshold voltages. As the gate voltage V_G is raised and approaches the threshold voltage V_T, three-dimensional effects become apparent. If the parasitic gate voltage V_{PG} is greater than the flatband voltage V_{FB}, then the onset of drain current now occurs at a lower gate voltage V_G with the formation of a corner region inversion layer. As the gate voltage is further increased, eventually, the inversion layer will spread under the entire gate. Once the MOSFET is fully turned on (V_G is much greater than V_T) the current is insensitive to the voltage V_{PG} applied to the parasitic gate.

The simulated I_D-V_G behavior for the conventional MOSFET under the influence of both the lateral and vertical parasitic MOSFETs is shown in Fig. 5, where the trench separates n- and p-channel devices with the n-substrate acting as the parasitic gate. In the simulation, the trench width was taken to be 1000 Å and the p-well to be uniformly doped to 10^{17} cm^{-3}. The solid line shows I_D as a function of V_G for the parasitic gate voltage V_{PG} equal to the flatband voltage V_{FB}. The bias conditions $V_{PG} > V_{FB}$ and $V_{PG} < V_{FB}$ are shown by the dashed and dotted lines, respectively. Due to 3-D effects, for $V_{PG} > V_{FB}$ the drain current in subthreshold increases to an unacceptable level, as much as 100 times higher than calculated from adding the currents from the conventional and parasitic MOSFETs, simulated individually. This is explained by the field enhancement in the corner region due to the parasitic gate. In contrast, for $V_{PG} < V_{FB}$, a higher gate voltage is required to invert the corner region due to the retarding field of the parasitic gate and, subsequently, the subthreshold current is reduced.

Finally, the 3-D effect is due mainly to the presence of the lateral parasitic MOSFET. For

most simulations, the interaction between the vertical parasitic MOSFET and the conventional MOSFET is minimal. In addition, including both parasitic MOSFETs in the simulation tends to be very CPU intensive and should be avoided. The total CPU time for each curve shown in Fig. 5, including both parasitic MOSFETs in the 3-D simulation, was approximately 8 hrs. on a Multiflow Trace 14/300, and required approximately 25 Mwords of memory for a grid consisting of 48,190 grid points. The simulation will run much faster if the dimensions of the grid are reduced by only including the lateral parasitic MOSFET and the conventional MOSFET in the 3-D simulation. The currents due to the vertical parasitic MOSFET can be calculated using 2-D simulation and added to the 3-D simulation results.

3 Corner Shielding Effect

In earlier work, where the trench width was taken to be 1 μm or greater, the I-V characteristics of the lateral parasitic MOSFET were determined by the conventional gate, not the parasitic gate. This effect is well known, generally known as either the narrow-width effect or inverse-narrow-width effect, depending on the topography of the isolation [6]. In Fig. 6(a), the mid-channel cross-section of a MOSFET is shown with the trench width of the order of 1 μm. At the channel edge, the fringing electric field of the conventional gate causes inversion along the region defined here to be the channel of the lateral parasitic MOSFET. It is only as the trench width is reduced below 0.5 μm that the parasitic gate cannot be ignored.

To study the interaction of the conventional and parasitic gate, the device structure corresponding to the cross-section shown in Fig. 6(b) was simulated, varying the trench width, the p-well doping N_W, and the gate extension W_{GE}. The trench width = 2500 Å, 5000 Å, gate extension W_{GE} = 0 Å, 1000 Å, and W_{GE} = *trench width*, and the p-well doping $N_W = 5\times10^{16}$ cm^{-3}, 1×10^{17} cm^{-3} were chosen to give a reasonable window of operation based on current process technology. The resulting leakage current, defined as the drain current I_D at V_G = 0V, is plotted in Figs. 7 and 8 as a function of the parasitic gate voltage V_{PG}. As shown in Fig. 7(a), at V_{PG} = 0V increasing the gate extension increases the drain current I_D, and increasing V_{PG} for fixed W_{GE} also increases the drain current I_D. In Fig. 7(b), the trench width is reduced, which also increases the leakage current. However, for a p-well doping of 1×10^{17} cm^{-3} and 5V on the parasitic gate, the leakage current is hardly worth considering, at less that 1 nA, even with the trench width reduced to 2500 Å. Decreasing the p-well doping to 5×10^{16} cm^{-3}, as shown in Fig. 8(b), with 5V on the parasitic gate, increases the leakage current to more than 0.1 μA. At these dimensions, bias conditions, and doping levels, the subthreshold leakage current is significant enough to degrade circuit performance.

As was shown in Figs. 7 and 8, the individual effects of the parasitic gate voltage and gate extension are to increase the subthreshold leakage current. However, as the voltage V_{PG} on the parasitic gate is raised, a crossover point is reached where an increase of the gate extension now reduces the leakage current. To explain this "peculiar" behavior we have to consider the distribution of the electric field lines shown for the device structure in Fig. 6(b). With the gate extended beyond the channel and the gate voltage at 0V, electric field lines from the parasitic gate now terminate on the gate extension instead of on the vertical sidewall of the MOSFET channel region. Thus the gate extension acts as a ground plane, shielding the corner region from the parasitic gate and reducing the leakage current for sufficiently large voltage V_{PG} on the parasitic gate. If the trench width is reduced, the influence of the gate extension increases as shown in Fig. 7(b), where the crossover point occurs at a lower parasitic gate voltage.

To illustrate the importance of the gate geometry, in Fig. 9 the leakage current at V_{PG}

= 0V, and 5V has been extracted from Figs. 7 and 8 as a function of gate extension W_{GE} for a trench width of 2500 Å. At V_{PG} = 0V, for p-well doping of 1×10^{17} cm^{-3}, the leakage current I_D varies by less than an order of magnitude and is well below the maximum leakage current tolerable. Even at V_{PG} = 5V, the variation over two orders of magnitude is unimportant because the leakage current is still below 10^{-9} A. However, when the p-well doping is reduced to 5×10^{16} cm^{-3}, the leakage current is considerably greater. But, we find that by varying the gate extension, the leakage current can be reduced to an acceptable level.

4 Conclusion

In this paper, we have shown that the leakage currents due to the 3-D effects not only depend on the isolation scheme, but also to a large extent on the topography of the gate electrode. It should now be clear that 1) technologically, the corner effect is very important because **the corner effect does not scale** and, thus, can produce a dramatic change in the *I-V* characteristics, which may pose serious problems for future scaling of the n^+ to p^+ spacing. And, in addition, 2) the recommended method of trench fill may depend on the leakage characteristics of the parasitic MOSFET. For instance, in the case where the trench is overfilled, the leakage current may be perhaps too large, but also may be significantly reduced when a planarization step is performed prior to the gate formation. Thus, the widely used method of trench fill must be re-examined carefully in conjuction with the gate electrode geometry.

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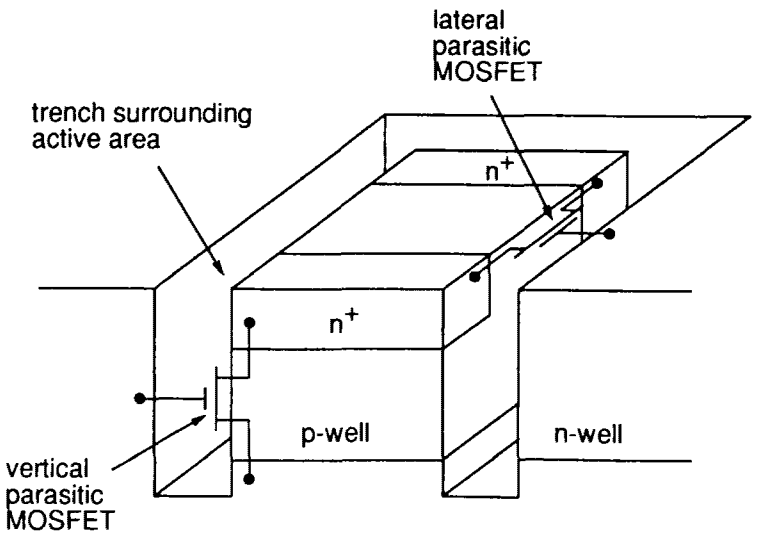


Figure 1: Schematic diagram of the BOX isolation technology illustrating the lateral and vertical parasitic MOSFETs [1].

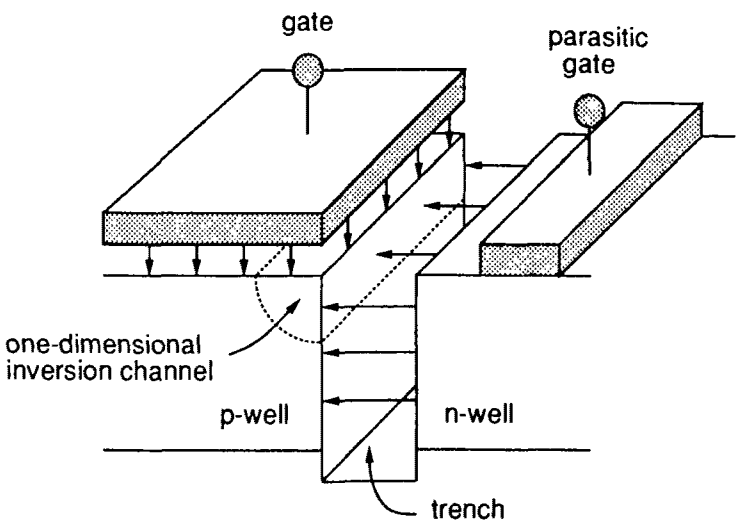


Figure 2: Three-dimensional "corner" effect. In subthreshold, the electric fields from the conventional and parasitic gate enhance each other, forming a one-dimensional inversion channel in the corner region where the gate and trench oxides meet.

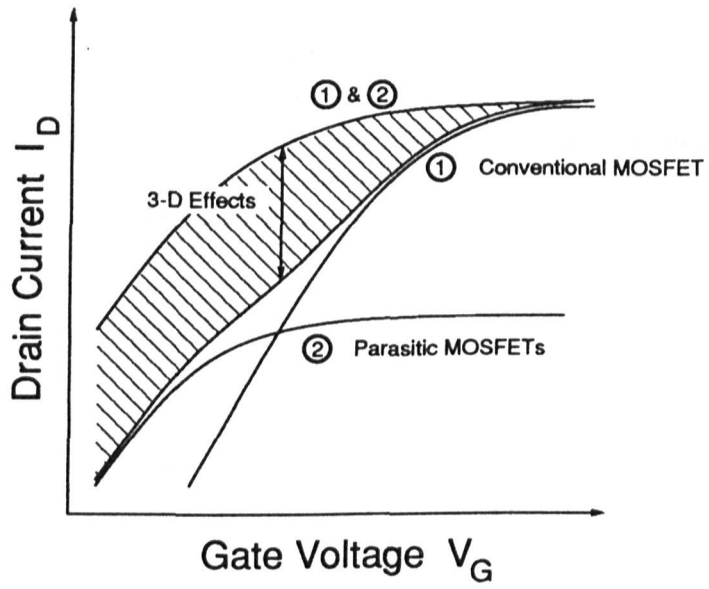


Figure 3: I_D-V_G behavior, shown qualitatively. Due to 3-D effects, the actual drain current I_D is significantly higher than predicted by adding together the drain currents from the conventional and parasitic MOSFETs, simulated individually.

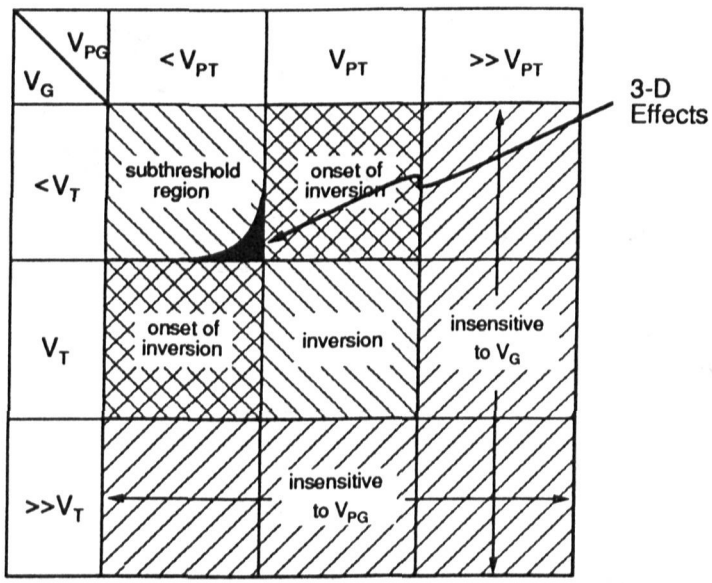


Figure 4: Table of the current modes as a function of the conventional and parasitic gate voltage V_G and V_{PG}.

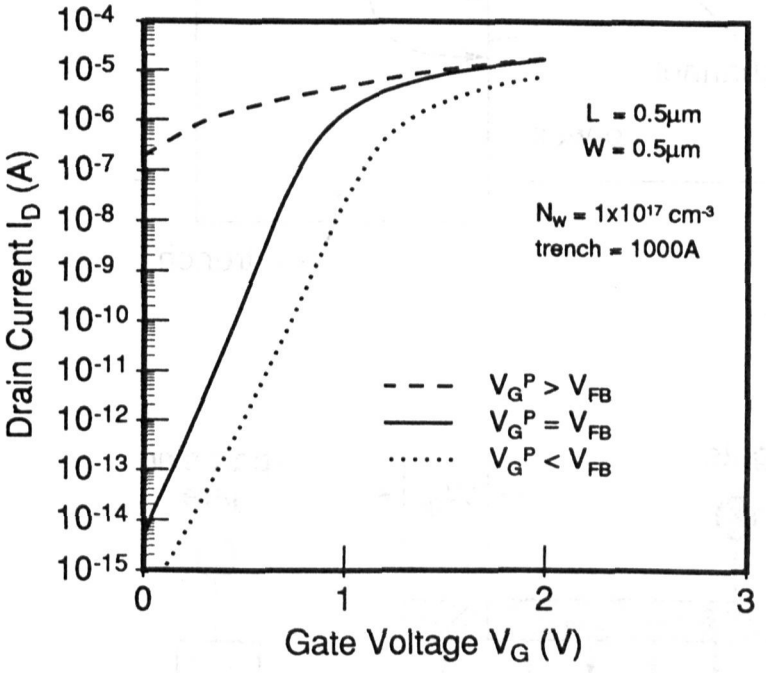
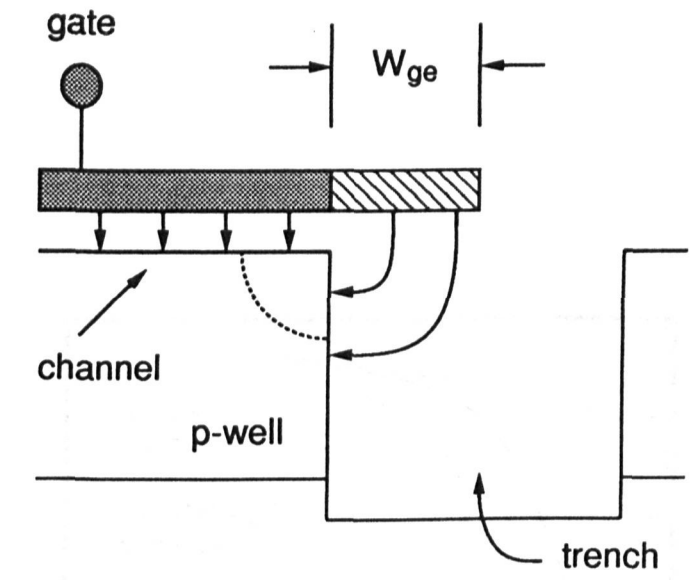
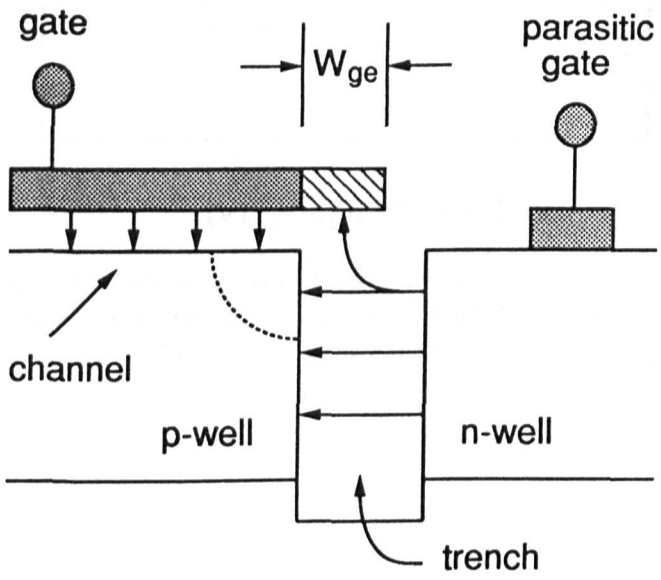


Figure 5: I_D-V_G behavior for the conventional MOSFET under the influence of the parasitic MOSFET. The dashed and dotted lines shows I_D-V_G for the parasitic gate voltage V_G^P = 4.0V, and -4.0V, respectively, where the flatband voltage V_{FB} = -0.96V.



(a)



(b)

Figure 6: Diagram of the electric field lines through a cross-section of the mid-channel for (a) wide trench, leading to the well known inverse-narrow-width effect, and (b) narrow trench, leading to the shielding effect described in the text and to reduced inverse-narrow-width effect.

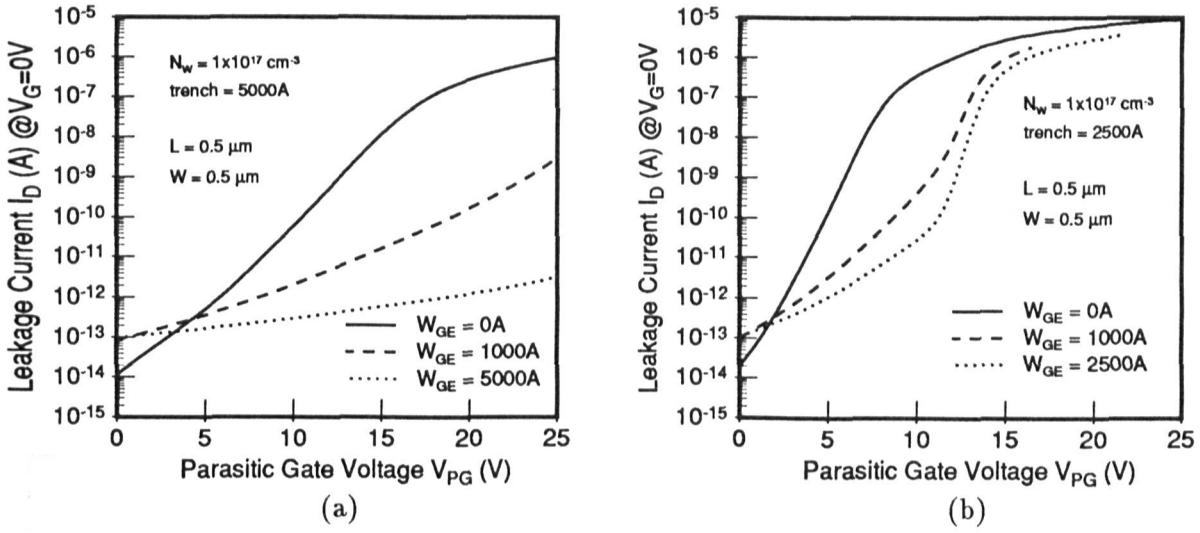


Figure 7: Dependence of the leakage current on parasitic gate voltage with gate extension over the trench as a parameter for uniform p-well concentration of 1×10^{17} cm^{-3}. (a) Trench width is 5000 Å, and (b) trench width is 2500 Å.

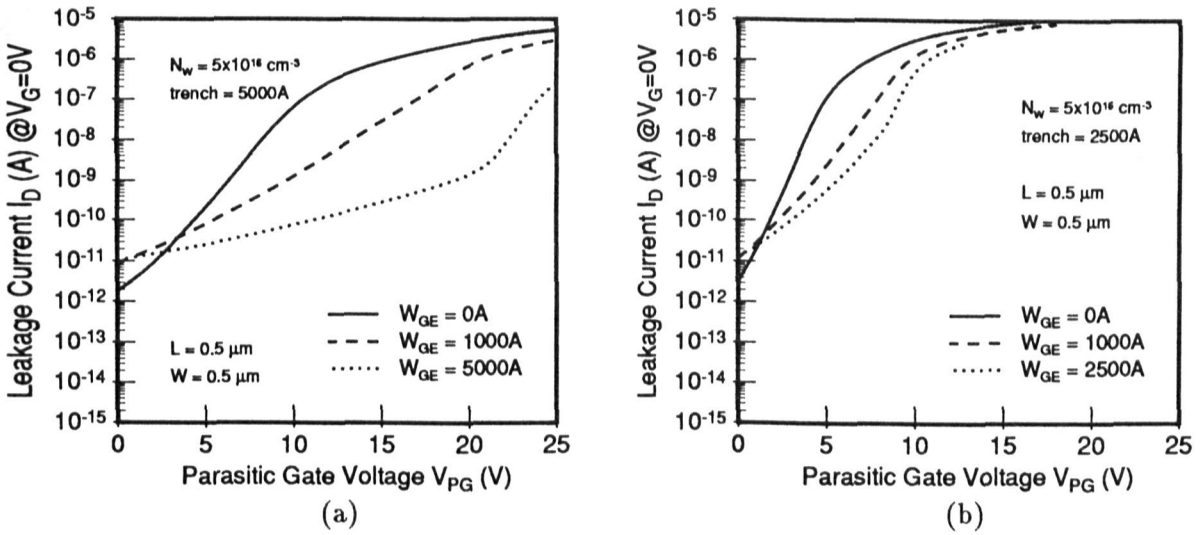


Figure 8: Dependence of the leakage current on parasitic gate voltage with gate extension over the trench as a parameter for uniform p-well concentration of 5×10^{16} cm^{-3}. (a) Trench width is 5000 Å, and (b) trench width is 2500 Å.

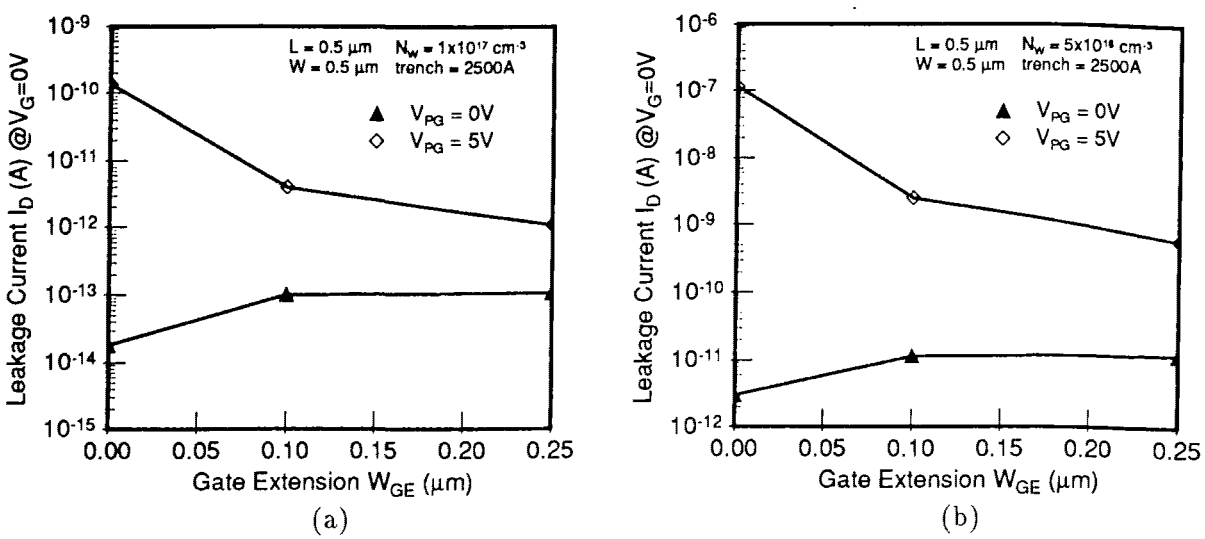


Figure 9: Leakage current as a function of the gate extension over the trench for two parasitic gate bias conditions $V_{PG} = 0, 5$V. (a) $N_W = 1\times10^{17}$ cm^{-3}, and (b) $N_W = 5\times10^{16}$ cm^{-3}.