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Three-Dimensional Device Simulation with Arbitrary Curved Boundaries using the Voronoi Discretization Method

Hitoshi Matsuo, Junko Tanaka, Akira Mishima*, Kazutami Tago*, and Toru Toyabe

Central Research Laboratory, Hitachi Ltd., Tokyo, Japan
Phone:+81-423-23-1111 Fax:+81-423-27-7699

*Energy Research Laboratory, Hitachi Ltd., Ibaraki, Japan
Phone:+81-294-53-3111 Fax:+81-294-53-2830

Abstract

A three dimensional device simulator that can simulate structures with arbitrary curved geometries has been developed. A boundary-fitted curvilinear coordinate system and the Voronoi polyhedron/prism discretization method are used in the 3D formulation. The narrow channel effect of MOS transistors is simulated within practical CPU time limits as an example .

1. Introduction

The miniaturization of devices in present ULSI technology often requires three-dimensional numerical tools to predict performance. Although a number of device simulators have been developed [1][2][3], many problems still remain. Since 3D simulations require huge amounts of computing resources, a sophisticated grid system suitable for representing arbitrary geometry is indispensable for practical simulation [4].

To simulate the characteristics of devices with arbitrary curved boundaries using a 3D drift-diffusion model, we introduce a novel three-dimensional boundary-fitted curvilinear coordinate system and a Voronoi discretization method.

2. Boundary-fitted Curvilinear Coordinate Grid Structure and Voronoi Polyhedron/prism Discretization

To represent arbitrary three-dimensional structures with a limited number of grid points, a boundary-fitted (BF) curvilinear coordinate system is adopted for geometric modeling. The generation of BF coordinates can be accomplished by numerically solving elliptic partial differential equations with the Dirichlet boundary conditions [5]. Figure 1 shows an example of a BF curvilinear coordinate system. To discretize this system, we expand a Voronoi polygon control volume [6] in 2D to a Voronoi polyhedron and a Voronoi prism as control volumes in 3D space. Figure 2(a) shows the Voronoi polyhedron control volume with 27 points of discretization.

In conventional rectangular 3D discretization grids, only 7 points are considered per control volume. The increase in discretization points in the Voronoi control volume, however, will not require too much additional computing and memory resources if the curved boundaries are not too complex. Many important effects can be simulated using grid structures that are partially linear in 3D space. For example, the narrow channel effect of MOSFET's can be simulated using a grid structure that is generated by sweeping a 2D grid along an auxiliarly-generated 1D grid. In order to optimize the number of discretization points, we also implemented 11 point discretization using the Voronoi prism control volume as shown in Figure 2(b).

At present, the discretized equations are solved using Gummel's decoupled method. The linearized system is solved by the CGS or BCG iterative linear solver.

3. Application to Narrow Channel Effects in MOSFET's

To demonstrate the efficiency of this three-dimensional formulation, we analyze the narrow channel effect in MOS transistors. Figure 3 shows the schematic view of a MOS transistor with LOCOS isolation. A p+ boron-doped region lies underneath the LOCOS as a channel stop. The curvilinear coordinate grid is generated by fitting the Si and SiO_2 boundaries. These grid points are concentrated at the interface where the inversion layer will form. Three channel widths (W/2 = 0.5μm, 1.0μm, 2.0μm) are selected to evaluate the

narrow channel effect, as shown in Figure 4. The total number of grid points for each MOSFET is 19x21x30 (=11970). The drain current versus drain voltage characteristics are shown in Figure 5. The threshold voltage, which is defined as the applied gate voltage when the drain current is 1nA, is plotted versus channel width in Figure 6. The increase in V_{th} for narrower channels due to boron channel-stop encroachment into the channel region is correctly predicted by the simulator.

The convergence properties of both the Voronoi polyhedron and Voronoi prism methods are compared in Figure 7. Although both methods require the same matrix elements, the electron continuity equation using 27 point discretization converges more rapidly than that using 11 points. This is because the matrix elements of the 27 point discretization can include some fill-ins during LU factorization. Total CPU time was 289 and 545 seconds for the two discretization methods for 17 bias voltage points on a Hitachi S-810 supercomputer (Table 1). In spite of the disadvantage in convergence, the 11 point discretization can reduce the CPU time to 53% compared to the 27 point discretization since a fewer number of points is involved in the calculations.

4. References

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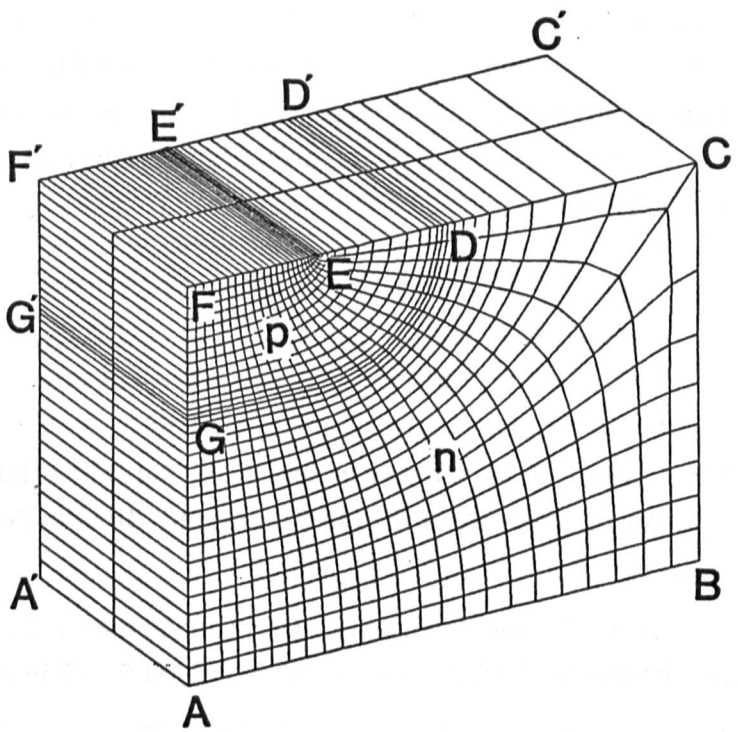
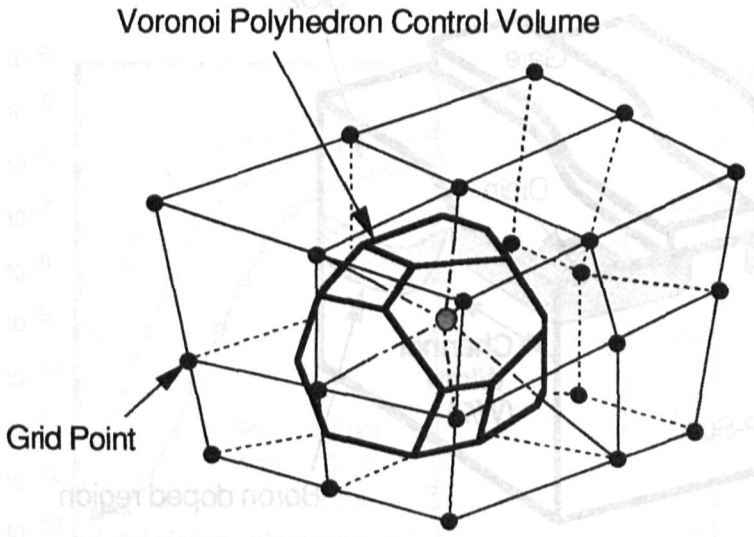
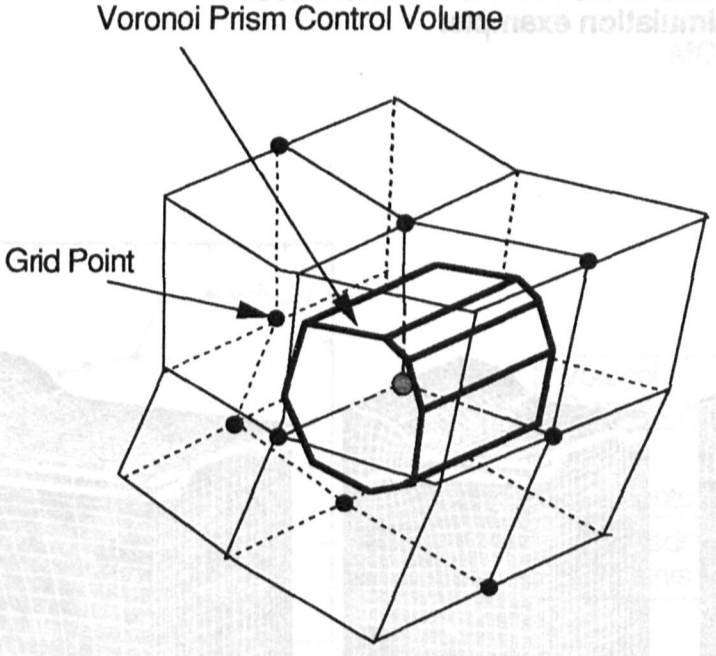


Fig.1 The curvilinear coordinate system.



(a) The Voronoi polyhedron control volume with 27-point discretization.



(b) The Voronoi prism control volume with 11-point discretization.

Fig.2 The Voronoi discretization method.

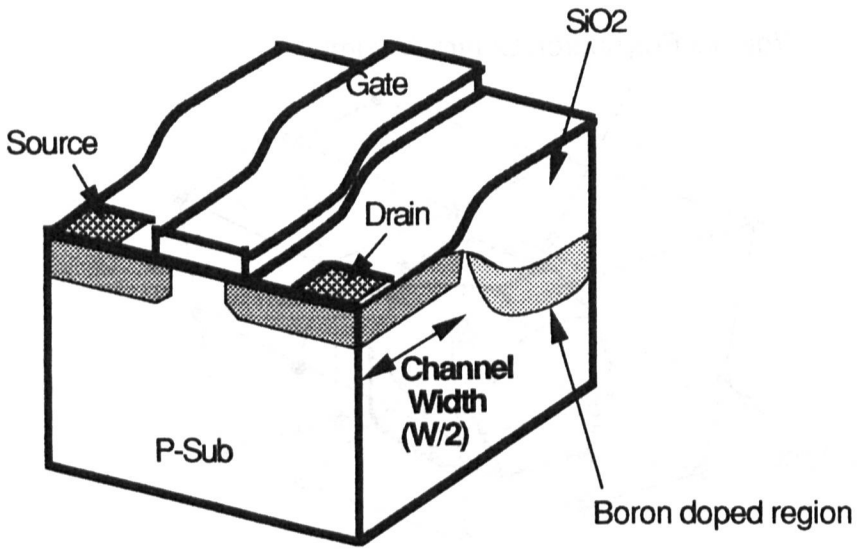
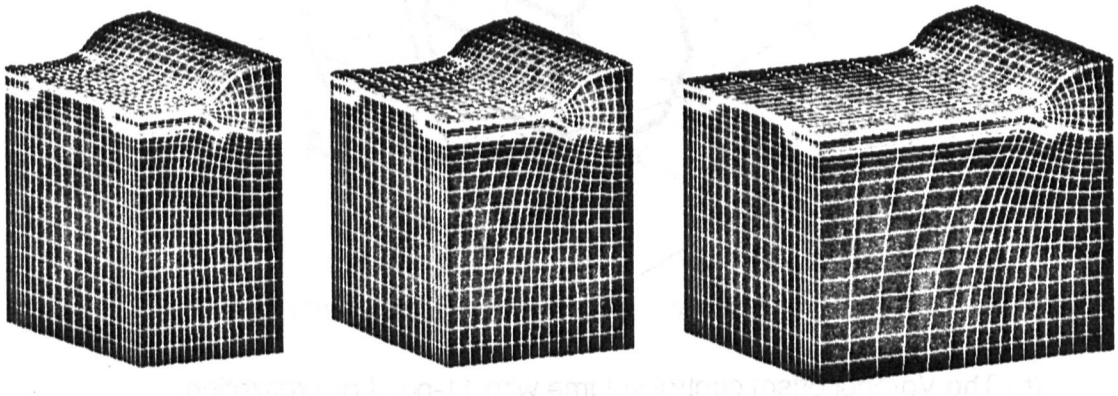


Fig.3 The three-dimensional MOSFET structure with LOCOS isolation used in the narrow channel effect simulation example.



W/2 = 0.5 μ m W/2 = 1.0 μ m W/2 = 2.0 μ m

Fig. 4 Grid structure of the simulated MOSFET's with LOCOS isolation.

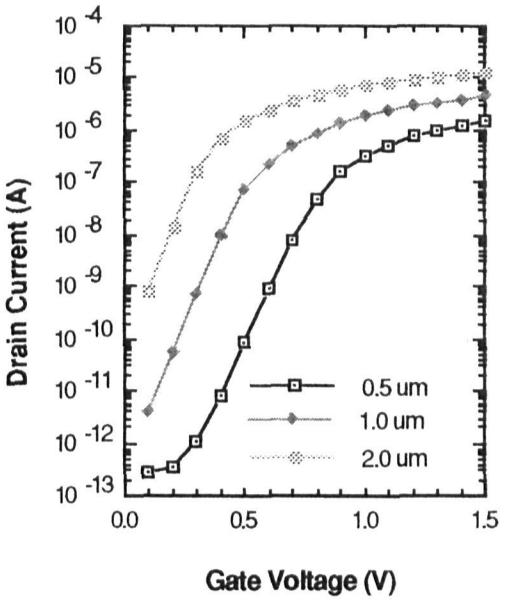


Fig. 5 Ids-Vds characteristics for the simulated MOSFET's.

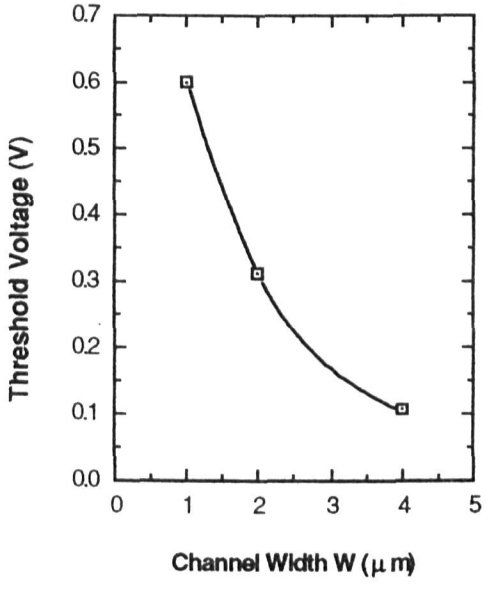


Fig. 6 Channel width dependence of the threshold voltage for the narrow channel MOSFET's.

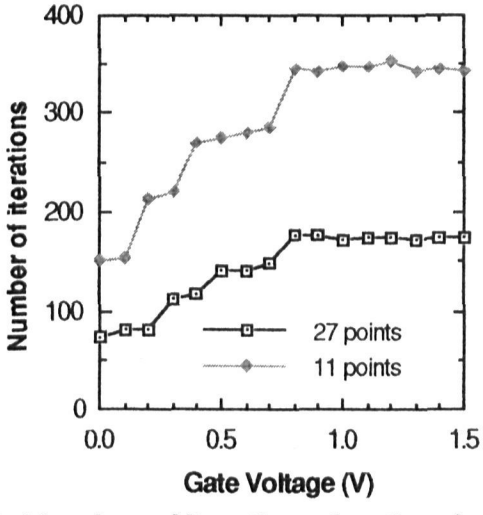


Fig. 7 Number of iterations for the electron continuity equation with 27-point and 11-point discretization.

Voronoi Discretization	CPU time (sec.)
Prism 11 points	289
Polyhedron 27 points	545

Table 1 Total CPU time for simulating the Ids-Vds characteristics with 17 bias points.