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Narrow-Channel Effect Simulation of Threshold Voltage and Channel-Conductance in Small MOSFET's Fabricated by LOCOS Process

Hiroo Masuda and
Hitachi, Ltd., 2326 Imai, Ohme-shi, Japan

Hitoshi Sugihara
Hitachi Ltd, Kodaira, Tokyo 187, Japan

Ryuichi Ikematsu
Hitachi Microcomputer Systems, Kodaira, Tokyo 187, Japan

Abstract

Small MOSFET's have been miniaturized in both terms of channel-length (L) and channel-width (W) within the range of a sub-micron in the VLSI memories. This paper describes the simulation and modeling of narrow channel devices focused on threshold voltage and channel conductance (gain factor). Three-dimensional simulation has been conducted on a device assuming the 1.3 um NMOS process with LOCOS isolation. Based on this simulation, an analytical equation for channel-potential distribution was approximated, which leads to new compact narrow-channel effect modeling of the device threshold and channel conductance. The proposed simple analytical model was verified by using NMOS fabricated with experimental 1.3 um CMOS technology. Narrow channel effect formulation was implemented into an MOS analytical model, and compared with experimental results. That the new model accommodated experimental I-V data well with an RSM error of less than 1 % for channel-length from 0.9 - 14.3 um was verified.

1. Numerical Simulation

The surface-potential distribution of narrow-channel devices has been studied based on a three-dimensional analysis. Device structure and bias conditions for the simulation are shown in Fig. 1. Here, gate-oxide thickness is 15 nm, substrate doping is $2x10^{16}$ cm^{-3}, LOCOS (birds-beak of 0.3 um) thickness is 0.5 um. Isolation doping is assumed to have a peak-density of 10^{18} cm^{-3} and a Gaussian profile with a standard deviation of 0.3 um. Total number of meshes is 39200. Computed results of surface potential and electron-density distributions are shown in Figs. 2 and 3. Figure 2 shows narrow channel effect on the device threshold (Vgs = 0.0 V, near-threshold). Conversely, Fig. 3 demonstrates narrow channel effect on device current gain characteristics.

The following physical implications on narrow channel effect in the LOCOS isolation processes can be assumed from these simulation results.

(1) Near-threshold bias conditions (Fig. 2)

Surface-potential distribution along the channel width deviates near the LOCOS edges of the channel. Surface potential decays exponentially at the LOCOS edges drastically, affecting carrier (electron) distribution. The resulting carrier density shows a Gaussian distribution

having a density peak in the middle of the channel (channel-width direction). It was noted that the device threshold can be determined by surface-potential in the middle of the channel.

(2) Strong-inversion conditions (Fig. 3)

Since the gate is biased during conditions of strong inversion, surface potential is leveled out more than under near threshold bias conditions. This also accumulates inversion charges into higher level of 10^{18} cm^{-3} or more. Simulated carrier density is divided under the two conditions, demonstrated by Fig. 3. These are the heavily inverted ones and moderately inverted ones at the LOCOS edges. Note that this carrier and potential distribution implies three parallel sub-transistors with a common gate, source and drain electrodes.

2. Modeling of Threshold Voltage

As demonstrated in Fig. 2, threshold voltage has to be determined based on surface-potential analysis in the channel-width direction. We assume potential distribution as shown in Fig. 4. The following equation is used as an analytical approximation of the curve, t.

$$\varphi_s(z) = \varphi_{so} - \eta_w\left(\exp\left(\frac{z - w_o/2}{\delta w/2}\right) + \exp\left(-\frac{z + w_o/2}{\delta w/2}\right)\right) \quad (1)$$

Where, z is the coordinate in the surface to channel width direction, w_O is effective channel width and δw is the characteristic width which determines edge effect by the LOCOS isolation layer. It is obvious that Eq. (1) shows a maximum value at z = wo/2 (center along the channel width).

$$\varphi_s(z)|_{max} = \varphi_{so} - \eta_w \exp\left(\frac{w_o}{\delta w}\right) \quad (2)$$

Since φ_{so} is the surface potential of the wide channel MOSFET, device threshold-voltage can be defined by a gate bias at which $\varphi_s(z)|_{max}$ reaches $B\phi f$ (B=2). Here, ϕf is the Fermi-voltage.

$$V_{th} = \varphi_{so} + K_b\sqrt{\varphi_{so} + |V_b|} \quad (3)$$

$$V_{th} = B\varphi_f + \eta_w \exp\left(\frac{w_o}{\delta w}\right) + K_b\sqrt{B\varphi_f + \eta_w \exp\left(\frac{w_o}{\delta w}\right) + |V_b|} \quad (4)$$

A convenient circuit model of the threshold voltage can be provided, if Eq. (4) can be divided into two parts which determine zero-bias (Vb = 0 V) threshold and effective back-gate bias constant.

Proposed approximate expressions for the above parameters are:

$$V_{to}(w_o) = V_{to} + \eta_{tw}\exp\left(-\frac{w_o}{\delta w}\right) \quad (5)$$

$$K_b(w_o) = K_{bo} + \eta_{bw}\exp\left(-\frac{w_o}{\delta w}\right) \quad (6)$$

It is of interest to notice that (1) the Vto and Kb show a similar narrow channel effect on their values and (2) both values can be formulated with an exponentially dependent function to effective channel width (w_o).

3. Modeling of Channel Conductance

As illustrated in Fig. 3, threshold voltage, along the channel-width direction, changes at the LOCOS edge. The simulation results show the validity of an assumption based on an equivalent model composed of with three parallel sub-NMOS's with a common gate, source and drain electrodes. Therefore, we have assumed an equivalent circuit for narrow channel operation under the strong inversion bias-conditions as shown in Fig. 5.

Based on this equivalent circuit, narrow channel effects on device parameters will be evaluated. A simplified drain current equation is analytically expressed as:

$$I_{ds} = \frac{w_o}{L}\frac{\beta_o}{1+\theta_e V_e}V_e^2 + \frac{\delta w}{L}\frac{\beta_o}{1+\theta_e(V_e-\delta)}(V_e-\delta)^2 \tag{7}$$

If we define an effective gate field factor $\theta e(eff)$ with the equation,

$$I_{ds} = \frac{w_o}{L}\frac{\beta_o}{1+\theta_e(eff)V_e}V_e^2 \tag{8}$$

The following equation is derived from Eqs. (7) and (8).

$$\frac{\beta_o}{1+\theta_e(eff)V_e} = \frac{\beta_o}{1+\theta_e V_e} + \frac{\delta w}{w_o}\frac{(1-\delta/V_e)^2}{1+\theta_e V_e(1-\delta/V_e)} \tag{9}$$

Using simple algebra and assuming $\delta << Ve$, one can derive the $\theta e(eff)$ - w_o relationship as:

$$\theta_e(eff) = \theta_e\left[1-\left(1+\frac{1}{\theta_e V_e}+\frac{1-\theta_e V_e}{1+\theta_e V_e}\left(\frac{\delta}{V_e}\right)\right)\left(\frac{\delta w}{w_o}\right)\right] \tag{10}$$

This equation indicates that (1) threshold reduction at the LOCOS edges results in a reduction of effective gate-field factor ($\theta e(eff)$) and (2) a reduction of θe, compared with the wide channel device, is inversely proportional to effective channel-width ($1/w_o$).

4. Experiments

NMOS's fabricated with experimental 1.3 um CMOS technology were measured to verify narrow channel effect in small MOSFET's. Experimental ΔVth, ΔKb - w_o curves are plotted on the semilog graph of Fig. 6. These results confirm the relationship shown in Eqs. (5) and

(6). Also, the gate-field factor of the devices is extracted from the experimental I - V curves of narrow channel devices. This result is shown in Fig. 7, showing reasonable agreement with theanalytical form of Eq. (10). The above formulations representing narrow channel effects on device parameters have been incorporated into an MOSFET model. Comparison of Ids - Vds characteristics between the improved model and experiments is shown in Fig. 8, showing a good correlation with an RMS error of less than 1 %, for NMOS devices with wo = 0.9 - 14.3 um.

5. Conclusions

Three-dimensional simulation has been conducted on a device assuming a 1.3 um NMOS process with LOCOS isolation. Based on the simulation, a new analytical-function for channel surface-potential was approximated, which led to the compact narrow channel effect modeling of device threshold and channel conductance. The proposed simple analytical models were verified by using NMOS fabricated with experimental 1.3 um CMOS technology. Narrow-channel effect formulation was implemented into an MOS analytical model, and compared with experimental Ids - Vds curves. That the new model accomodated experimental I-V data well, with an RMS error of less than 1 %, on devices with channel-width of 0.9 - 14.3 um was verified.

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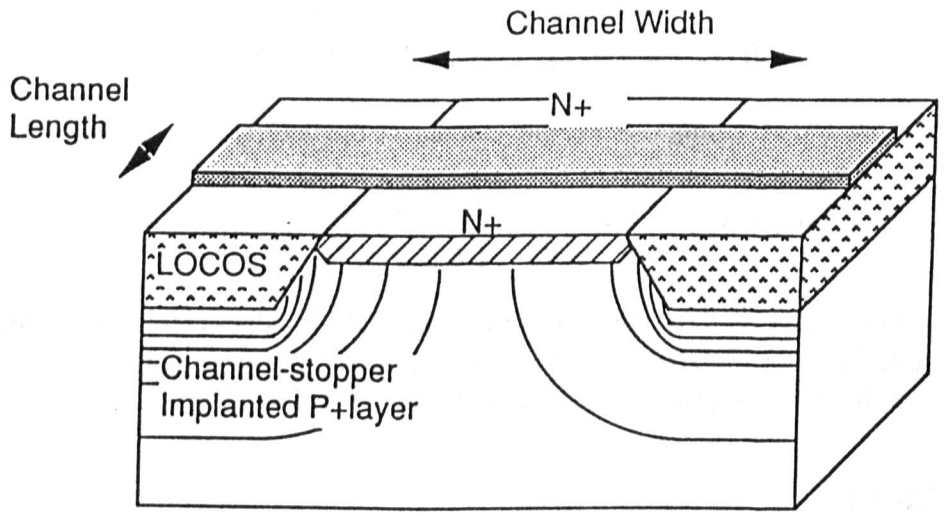

Fig. 1 Three-dimensional simulation device structure for narrow-channel effect.

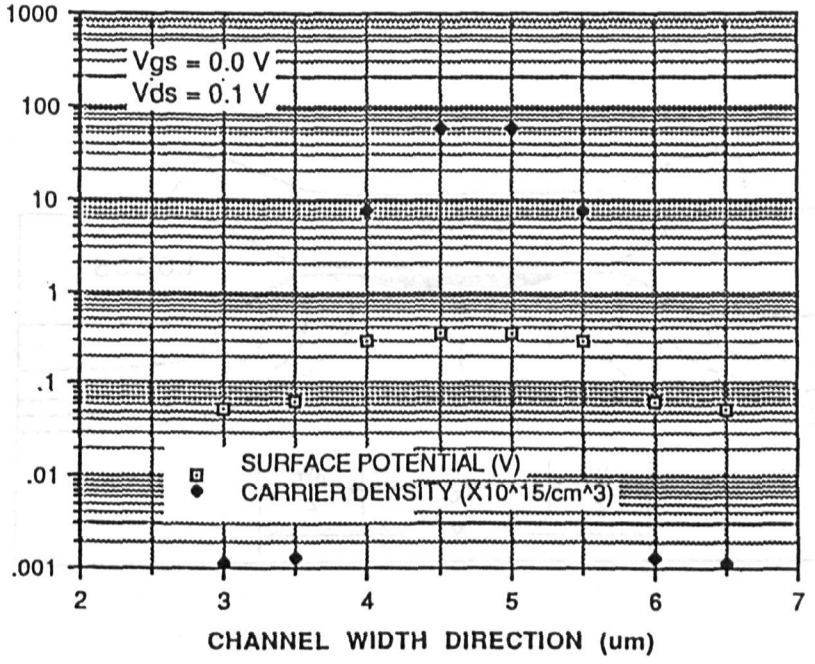

Fig. 2 Computed potential and carrier density distributions along channel width direction.

(Vgs=0V, Vds=0.1V)

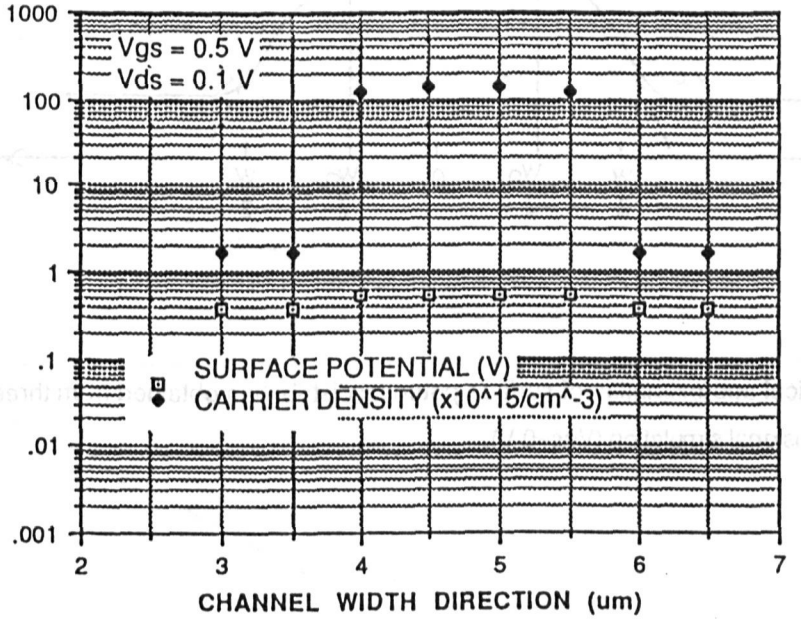

Fig. 3 Computed potential and carrier density distributions along channel width direction.

(Vgs=0.5V, Vds=0.1V)

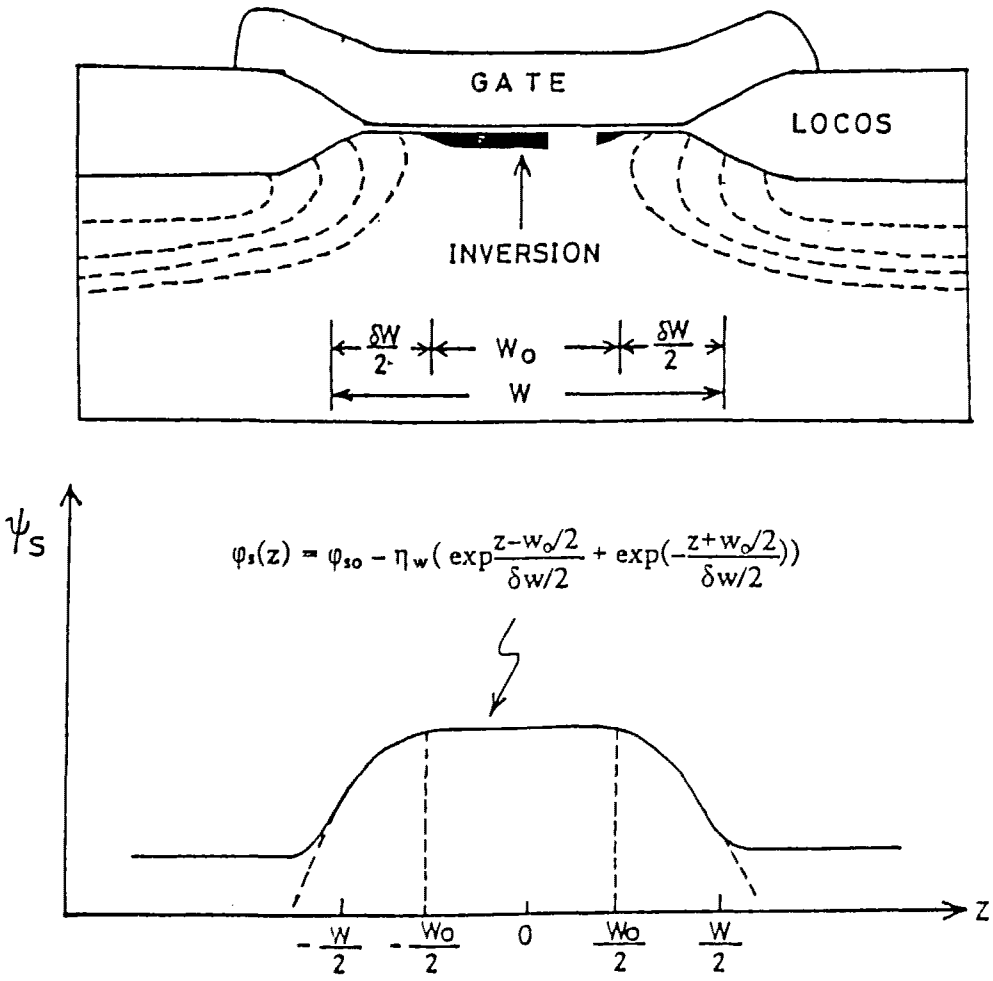

Fig. 4 Analytical approximation of surface-potential distribution obtained from three-dimensional simulation (Vgs=0 V).

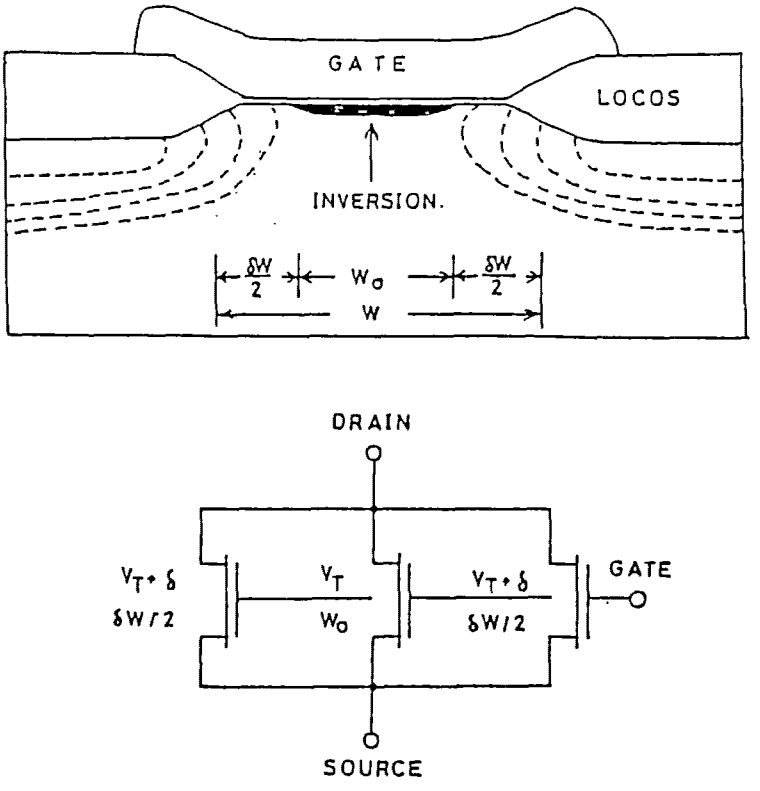

Fig. 5 Equivalent transistor model of narrow-channel operation under strong-inversion conditions.

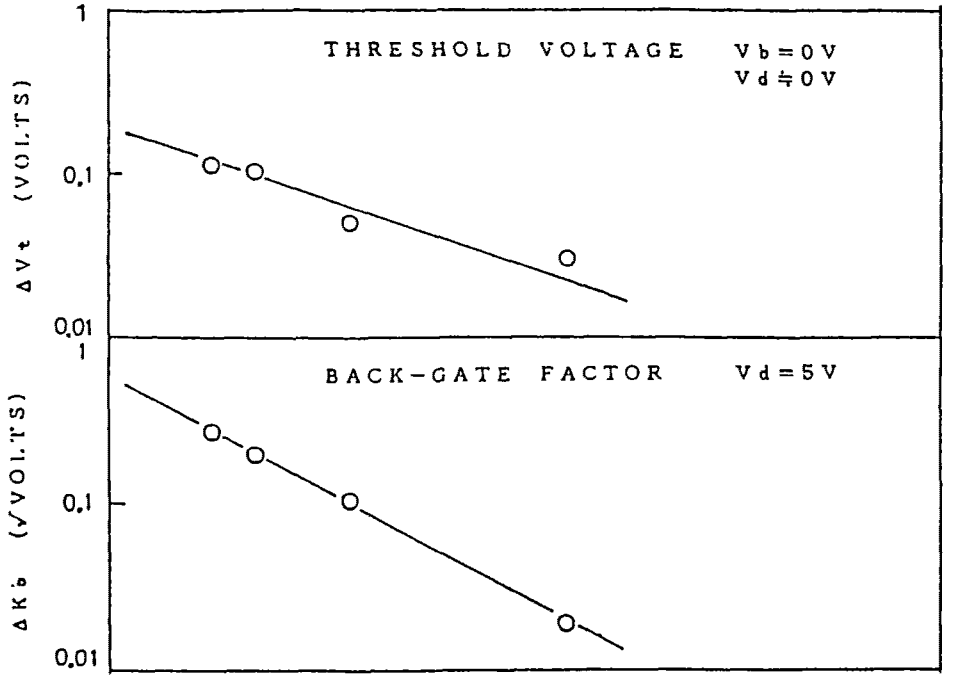

Fig. 6 Comparison of ΔVth- and ΔKb-W characteristics between proposed model and experimental results.

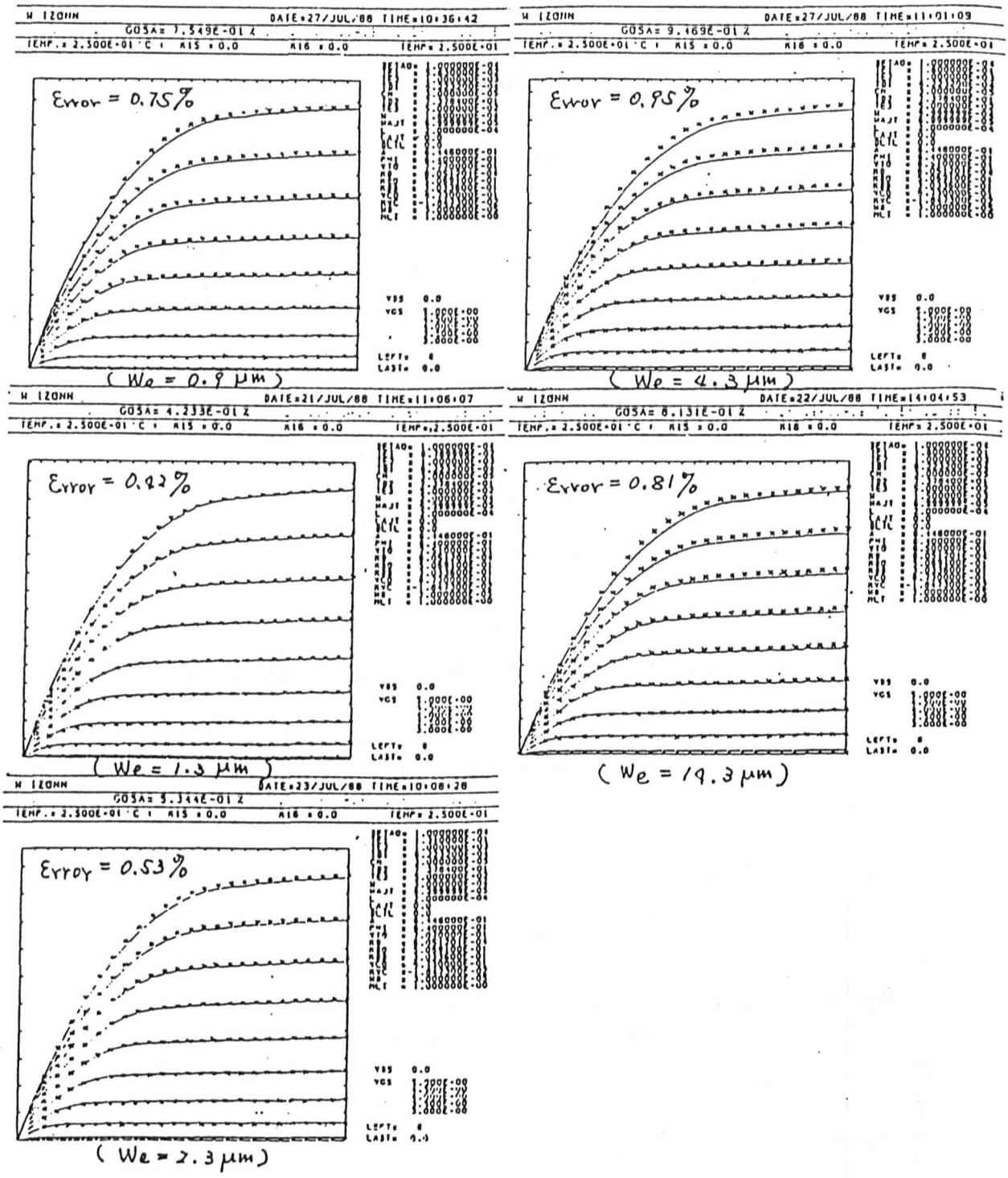

Fig. 7 Comparison of Ids-Vds characteristics, on devices with W=0.9~14.3 um, between narrow-channel effect compact models and experimental results.