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Latch-up Prevention in Merged Bipolar-MOS Structures for BiCMOS Applications

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Abstract

A two-dimensional numerical simulation study of latch-up and its prevention in merged bipolar-MOS structures for BiCMOS applications is presented in this paper. Techniques to enhance latch-up immunity of the structures are proposed.

1. Introduction

BiCMOS technology [1] offers both the high driving capability of bipolar devices and the high input impedance of CMOS devices. The potential of BiCMOS technology has been demonstrated in a variety of applications such as gate arrays [2], static RAMs [3], dynamic RAMs [4] and microprocessors [5].

One of drawbacks of the conventional BiCMOS process is that the integration density is rather low since the MOS and bipolar devices are built in separate islands and interconnected externally. Furthermore, parasitic interconnect capacitance and resistance may cause substantial delay during transient operation. To overcome these problems, the use of physically merged bipolar-MOS devices in the implementation of BiCMOS circuits have been proposed [6-10]. Fig. 1 shows a complementary BiCMOS inverter circuit. The pull-up and pull-down transistors are a merged PMOS and NPN structure (BiPMOS) and a merged NMOS and PNP structure (BiNMOS).

The merged structures, however, involve a parasitic bipolar device, which may cause latch-up. Therefore, the stability of the structures and of the overall circuits is of major concern in the design of the BiCMOS circuits and systems. No approprate technique for latch-up prevention in these structures has been reported in the literature as yet. In this paper, a more detailed discussion of latch-up and an investigation of latch-up prevention in merged BiCMOS structures using two-dimensional simulations are presented. A latch-up free structure is proposed.

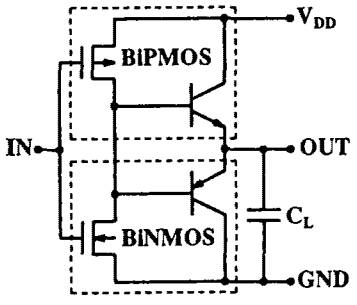

Fig. 1. Schematic diagram of a physically merged BiCMOS inverter.

2. Latch-up in the Merged BiCMOS Circuit

There are two kinds of latch-up in merged BiCMOS circuits. The first is the latch-up between the n-channel and the p-channel devices, commonly encountered in CMOS circuits. The second is the latch-up in each individual merged BiPMOS or BiNMOS device. A BiCMOS circuit will only operate properly if both forms of the latch-up are prevented. The objective of this paper is to investigate and find methods to prevent the second form of latch-up inherent in the merged devices.

Fig. 2(a) and (b) illustrate the basic structure and the equivalent circuit of the BiPMOS and BiNMOS merged devices. In the BiPMOS, shown in Fig. 2(a), Q_N and M_P are the merged devices. Q'_P is the lateral parasitic device underneath the gate. R_C is the series collector resistance formed by the n-well, the n^+ buried layer and the deep n^+ collector contact diffusion. When the collector current of Q_N is sufficiently high, the voltage drop across R_C turns Q'_P on and the BiPMOS structure latchs. Similar latch-up can also occur in the BiNMOS structure.

3. Device Simulation

A process simulator (TMA SUPREM-3) [11] was used to design the fabrication process for the merged structures. The simulated doping profiles were used as input to a two-dimensional device simulator (TMA PISCES-2B) [12] to characterize the performance of the structures.

3.1. Latch-up Simulation of the Merged Structures

The structures shown in Fig. 2 were simulated. The gate oxide thickness was 200 Å and the effective gate length was 0.8 μm. The threshold voltages V_{th} of M_P and M_N were –0.6V and 0.6V, respectively. The thickness of the polysilicon emitter layer was 0.25 μm. The maximum current gain β_{max} of the vertical bipolar transistors Q_N and Q_P was 110. The peak doping concentration for the n^+ and p^+ buried layer was 5×10^{18} cm^{-3}. The simulated emitter current I_E versus emitter to source

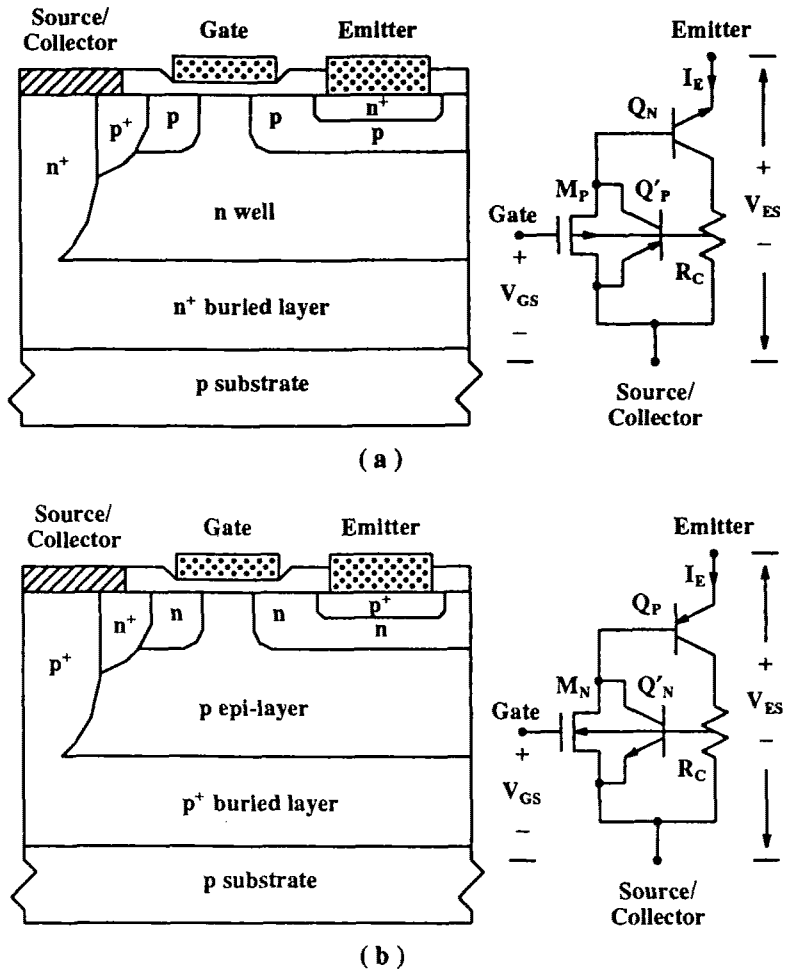

Fig. 2. Basic structure and equivalent circuit of (a) BiPMOS and (b) BiNMOS devices.

voltage V_{ES} for the structures is shown in Fig. 3. Latch-up in the merged structures is observed. The latch-up voltages are –3.2V at V_{GS}=–5V and 2.1V at V_{GS}=5V for the BiPMOS and BiNMOS, respectively.

3.2. Latch-up Prevention

(a) BiPMOS Structure

Conduction in the lateral parasitic transistor Q'_P in the merged BiPMOS structure causes the latch-up of the structure. If the parasitic transistor is prevented from turning on, latch-up can be prevented. In [8], a negative feedback technique was used to reverse bias the emitter-base junction of Q'_P. Although the latch-up was prevented, the negative feedback resulted in a decrease in the device

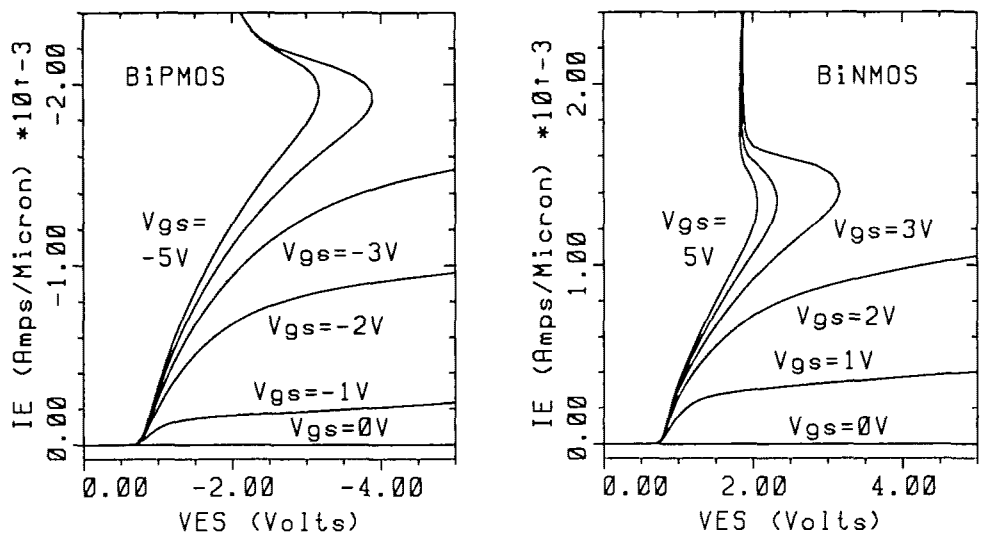

Fig. 3. Simulated I_E-V_{ES} characteristics of the BiPMOS and BiNMOS structures.

current handling capability.

Alternatively, if the collector series resistance R_C, in Fig. 2(a), is sufficiently low, the voltage drop cross R_C is low and the turn-on conditions for Q'_P can be eliminated. An increase in the doping concentration for the n^+ buried layer will result in a reduction of R_C. Fig. 4 shows the I_E-V_{ES} curves at V_{GS}=–5V for BiPMOSs with different buried layer doping concentrations. As can be seen, the latch-up voltage increases with the buried layer doping. For the structure with a 5×10^{19} cm^{-3} n^+ buried layer, the latch-up voltage is higher than –10V. Therefore, to prevent latch-up in the BiPMOS structure, the n^+ buried layer doping concentration should be as high as possible and should not be lower than 5×10^{19} cm^{-3}.

(b) BiNMOS Structure

Due to out diffusion of boron, which is the only dopant can be used, from the p^+ buried layer in the BiNMOS structure, the maximum doping concentration for that layer is limited to around 5×10^{18} cm^{-3}. The collector series resistance R_C is relatively high. The parasitic bipolar transistor in the structure is a NPN device Q'_N. This device usually has a larger current gain than the parasitic PNP in the merged BiPMOS structure. Latch-up problems in the merged BiNMOS structure are therefore more severe.

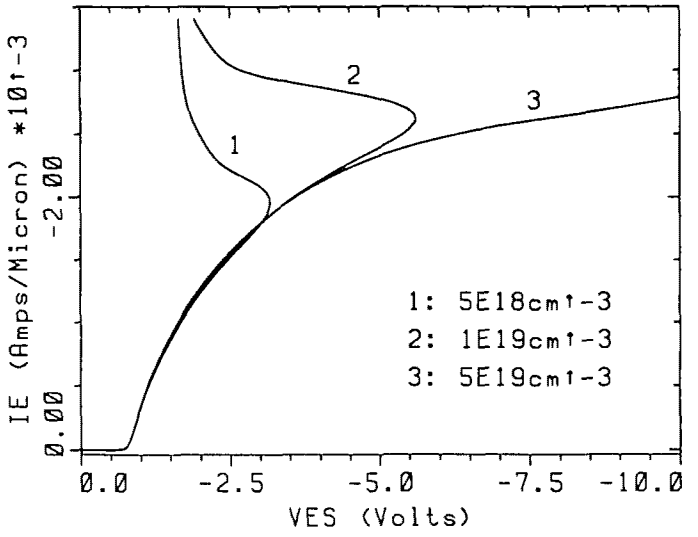

Fig. 4. Simulated I_E-V_{ES} characteristics as a function of n^+ buried layer doping concentration at V_{GS}=–5V for the BiPMOS structure.

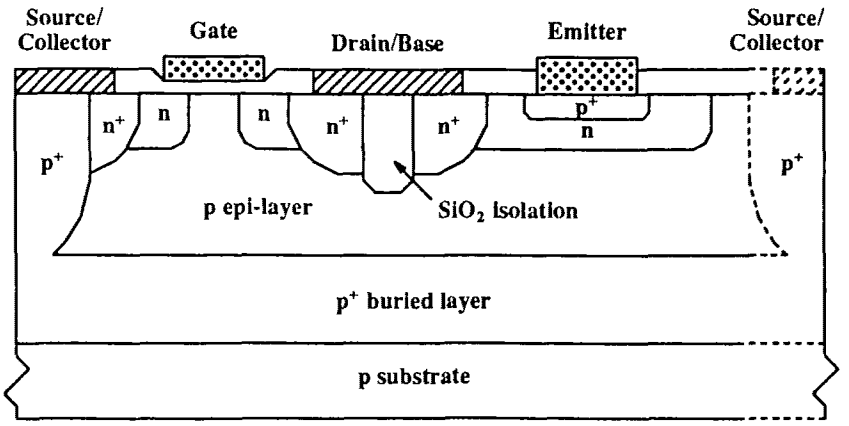

Fig. 5. Structure of SiO_2 isolated BiNMOS device.

To prevent latch-up in such a structure, a simple modification structure involving SiO_2 isolation is proposed. Fig. 5 shows the cross sectional view of the SiO_2 isolated merged BiNMOS structure. The SiO_2 region is used to block the latch-up path inherent in the structure. Also shown in the dashed lines is a second source/collector contact used to reduce the collector resistance R_C and to increase the latch-up voltage of the structure even further.

The SiO_2 isolated BiNMOS structure was simulated. The SiO_2 region was deeper than the n^+ drain/base contact. In the present case, this depth was 0.6μm. The peak doping concentration for the p^+ buried layer was varied from 1×10^{18} cm^{-3} to 5×10^{18} cm^{-3}. Fig. 6 shows the simulated I_E-V_{ES} characteristics at V_{GS}=5V for the BiNMOSs with and without the second source/collector contact. For structures without the second source/collector contact, the maximum latch-up voltage obtained is around 5.5V. For structures with the second source/collector contact, the structure is latch-up free up to 10V if the doping for the buried layer is higher than 1×10^{18} cm^{-3}. In applications where high latch-up voltage is required, using two source/collector contacts is the preferred choice. The penalty in increased device area is about 15%.

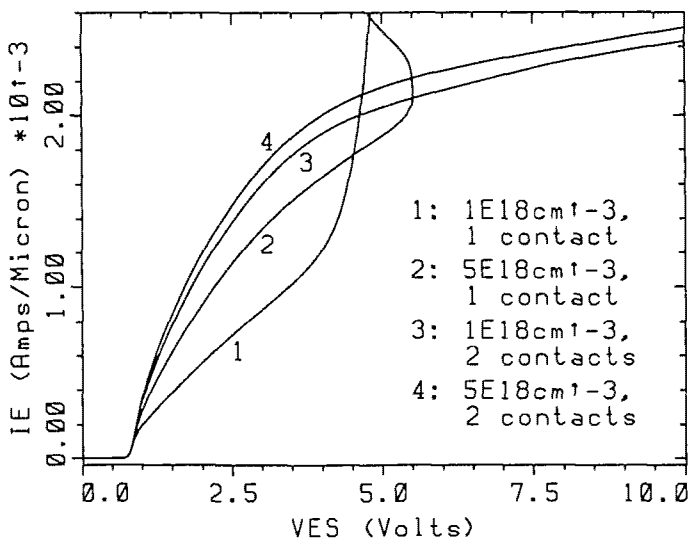

Fig. 6. Simulated I_E-V_{ES} characteristics as a function of p^+ buried layer doping concentration at V_{GS}=5V for the SiO_2 isolated BiNMOS structure.

For comparison purposes, BiNMOS structures without the SiO_2 isolation but with the same p^+ buried layer were also simulated. Latch-up free operation was not achieved even when two source/collector contacts were used.

4. Conclusion

Two-dimensional simulations related to latch-up prevention in the merged bipolar-MOS devices were performed. It was found that the latch-up can be prevented by proper design of the device. To design latch-up free BiPMOS structures, the buried layer doping concentration must be higher than 5

$\times 10^{19}$ cm^{-3}. A SiO_2 isolation technique and a second source contact were proposed to enhance the latch-up immunity of the BiNMOS structure.

Acknowledgements

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