*SIMULATION OF SEMICONDUCTOR DEVICES AND PROCESSES Vol. 4*
*Edited by W. Fichtner, D. Aemmer - Zurich (Switzerland) September 12-14, 1991 - Hartung-Gorre*



# Two-Dimensional Simulations of AlGaAs/GaAs HBTs with Various Collector Structures

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## Abstract

Cutoff frequency characteristics of AlGaAs/GaAs HBTs with various collector structures are studied by two-dimensional simulation. Thinner $n^-$-collector layer with higher doping density is desirable to achieve higher cutoff frequency. Possible merit and demerit caused by introducing semi-insulating external collectors are also discussed.

## I. Introduction

Recently, AlGaAs/GaAs heterojunction bipolar transistors (HBTs) have received great interest for application to high-speed and high-frequency devices.[1] Reduction in the collector delay time is very important in achieving higher cutoff frequencies of the HBTs.[2] Other delays such as the emitter charging time and the base transit time can be minimized by increasing collector current and by introducing a graded-bandgap base. To reduce the parasitic base-collector capacitance and to improve the high-frequency performance, semi-insulating external collectors are often introduced.[3),4] They are realized by oxgen or proton implantation. However, it is not well clarified how the semi-insulating layers affect device characteristics.

In order to predict device characteristics or to optimize device design, many one-dimensional simulations of AlGaAs/GaAs HBTs have been made[5)-8)], and some of them treat electron transport in the collector layer.[7),8)] However, one-dimensional approaches can't include effects of external base-collector junctions. Several two-dimensional simulations of AlGaAs/GaAs HBTs have also been made[9)-11)], but most of them concentrate on problems about the emitter-base junctions and the base layer.

In this work, we have made two-dimensional simulations of AlGaAs/GaAs HBTs with various collector structures and studied design criteria for the collector layer. In addition, possible merit and demerit caused by introducing semi-insulating external collectors are also discussed.

## II. Physical Model

Device structures simulated in this study are shown in Fig.1. A graded bandgap base is introduced. (a) is a structure with a usual $n^-$ external collector, where the donor density $N_{C1}$ is varied from $10^{16}cm^{-3}$ to $10^{17}cm^{-3}$, and its thickness $L_{C1}$ is varied from 0.1 μm to 0.7 μm. (b) is a structure with a semi-insulating external collector, where $N_{C1}$ and $L_{C1}$ are set to $5x10^{16}cm^{-3}$ and 0.5 μm, respectively. Here we assume that the semi-insulating (i) layer is achieved by introducing a deep acceptor into the $n^-$-layer. Its density $N_T$ must be higher than $N_{C1}$. We also assume that the deep acceptor is at the midgap. Electron and hole capture cross sections of the deep acceptor are typically set to $10^{-18}cm^2$ and $10^{-16}cm^2$, respectively.

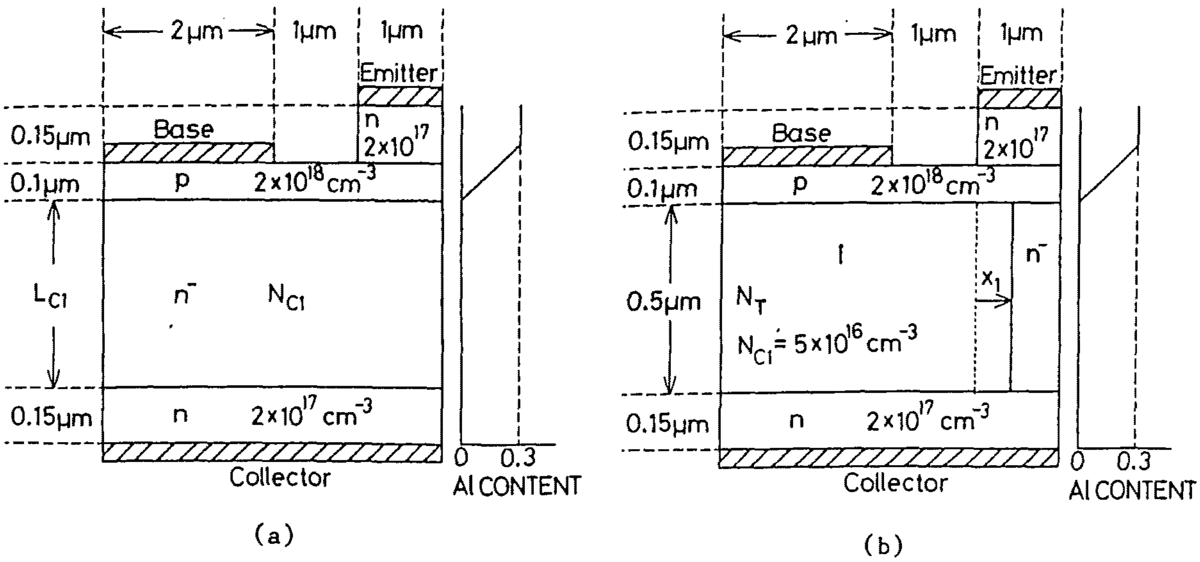


Fig.1 Device structures simulated in this study.
(a) HBT with $n^-$-collector thickness of $L_{C1}$ and $n^-$-doping density of $N_{C1}$.
(b) HBT with semi-insulating external collector.

Basic equations are the Poisson's equation including the ionized deep-acceptor term, continuity equations for electrons and holes, and current equations for electrons and holes.[12] In the continuity equations, an additional recombination rate via the deep acceptor is included. Material parameters used in this study are similar to those used in a previous study.[8] The basic equations are put into discrete forms by the finite difference method and solved by a decoupled method.

In this study, we concentrate our attention on how small-signal parameters such as cutoff frequency $f_T$ and collector delay time $\tau_C$ are affected by collector structures. The deep acceptor is handled during small-signal parameter extraction by the following way: holding its concentration fixed during the small-signal swing to obtain the high-frequency performance.[13),14] $f_T$ and $\tau_C$ are calculated by the following equations.

$$f_T = \frac{1}{2\pi} \cdot \left. \frac{\partial I_C}{\partial Q_n} \right|_{V_{CE} = \text{const.}} \tag{1}$$

$$\tau_C = \left. \frac{\partial Q_{nC}}{\partial I_C} \right|_{V_{CE} = \text{const.}} \tag{2}$$

where $Q_n$ and $Q_{nC}$ are electron charges in the whole device and in the collector region, respectively, $I_C$ is the collector current density (normarized by emitter area), and $V_{CE}$ is the collector-emitter voltage.

## III. Results and Discussions

### A. Dependence of $f_T$ on $n^-$-Collector Parameters

First, we describe cutoff frequency characteristics of HBTs with a ususal $n^-$ external collector shown in Fig.1(a).

Fig.2 shows calculated cutoff frequency $f_T$ versus collector current density $I_C$ curves as a parameter of donor density in the $n^-$-collector layer $N_{C1}$. For higher $N_{C1}$, achievable $f_T$ is higher in the high $I_C$ region because $\tau_C$ becomes shorter, though $f_T$ is lower in the relatively low $I_C$ region as a result of longer $\tau_C$. For higher $N_{C1}$, the thickness of collector depletion layer should be thinner[8], leading to a shorter collector transit time and a longer collector charging time. In the high $I_C$ region, the charging time decreases and hence the transit time becomes important. Therefore, above results imply that when a cutoff frequency is considered, reduction in the collector transit time is more important than reduction in the collector charging time.

Fig.3 shows $f_T$ - $I_C$ curves as a parameter of the thickness of $n^-$-collector layer $L_{C1}$. For shorter $L_{C1}$, achievable $f_T$ is higher. This is because for shorter $L_{C1}$, the thickness of collector depletion layer is thinner, resulting in a shorter transit time in this region.

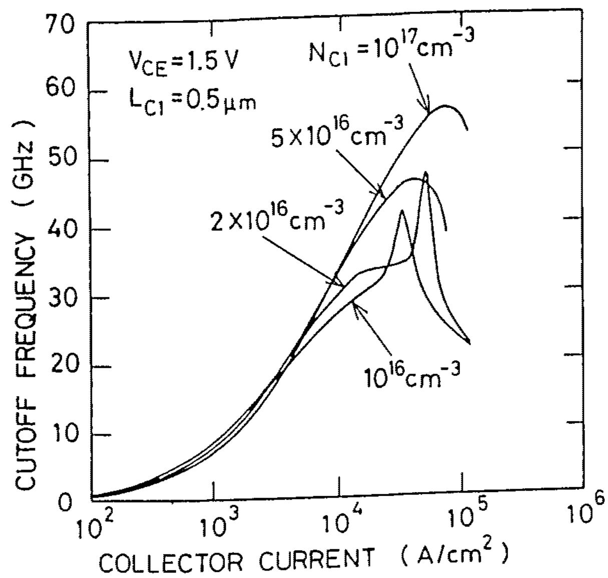


Fig.2 Cutoff frequency $f_T$ versus collector current density $I_C$ curves for HBTs with $L_{C1}$ = 0.5 μm, with $N_{C1}$ as a parameter. Collector-emitter voltage $V_{CE}$ = 1.5 V.

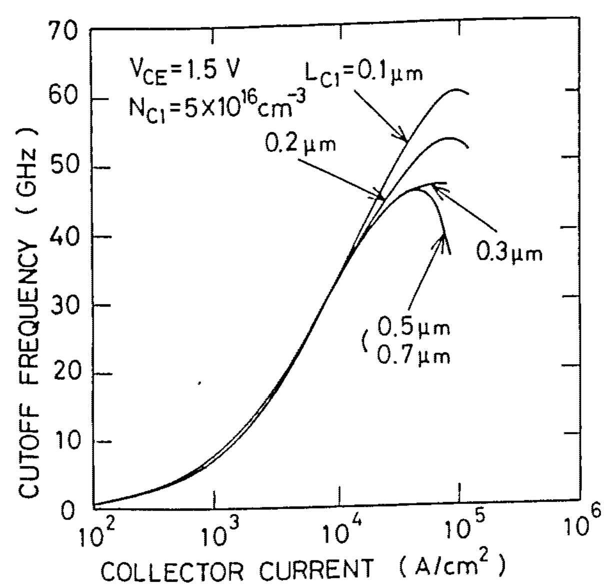


Fig.3 $f_T$ versus $I_C$ curves for HBTs with $N_{C1}$ = $5\times10^{16}cm^{-3}$, with $L_{C1}$ as a parameter.

From above results, we can say that to achieve higher $f_T$, reduction in the collector transit time is important, and for this purpose, $N_{C1}$ should be designed higher and $L_{C1}$ should be designed thinner.

## B. Effects of Introducing Semi-insulating External Collectors

Next, to investigate effects of introducing semi-insulating external collectors, we have calculated cutoff frequency characteristics of HBTs with different $x_1$ in Fig.1(b). Positive $x_1$ means that the semi-insulating layer extends into the intrinsic collector region, while negative $x_1$ means that the semi-insulating layer is away from the intrinsic collector region.

Fig.4 shows examples of calculated $f_T$ - $I_C$ curves as a parameter of $x_1$. For reference, a case of $N_T$ = 0 and a case of one-dimensional structure are also shown. $N_T$ = 0 corresponds to a case with a usual $n^-$ external collector. Fig.5 shows the maximum value of $f_T$ in each $f_T$ - $I_C$ curves, $f_{Tmax}$, as a function of $x_1$. From these figures, we can see that by introducing the semi-insulating external collector, $f_T$ improves in the low $I_C$ region as expected, but it begins to decrease earlier in the high current region and an achievable $f_T$ becomes lower (when $x_1 \geq 0$) than for a case without i-layer ($N_T$ = 0). This is an unexpected result.

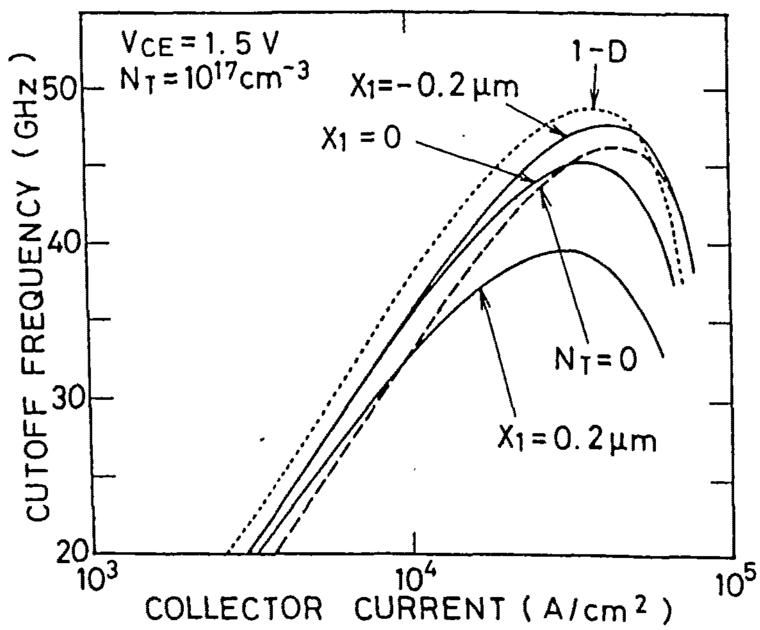


Fig.4 $f_T$ versus $I_C$ curves for HBTs with semi-insulating layer shown in Fig.1(b) ($N_T$ = $10^{17}$ $cm^{-3}$), with $x_1$ as a parameter.

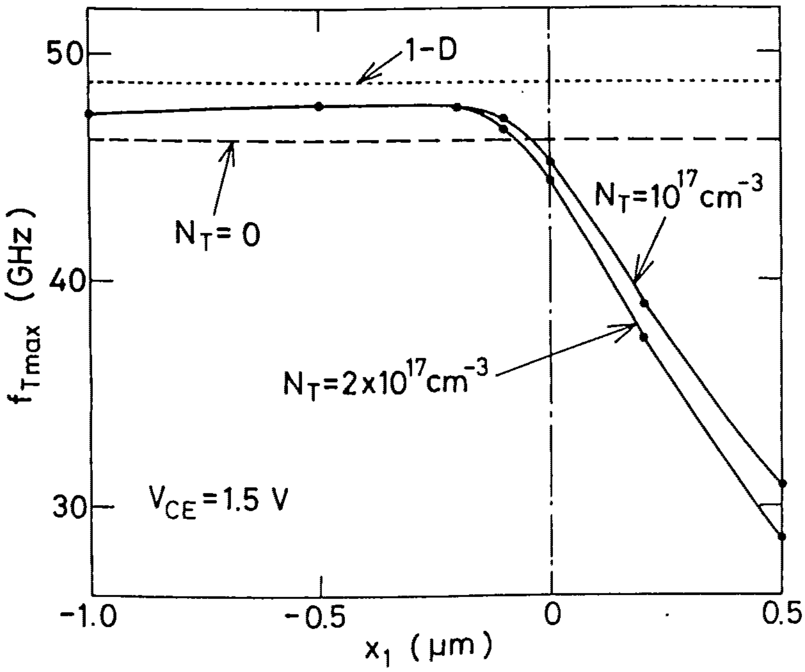


Fig.5 Maximum value of cutoff frequency in $f_T$ - $I_C$ curves, $f_{Tmax}$, as a function of $x_1$.

To consider above points further, we introduce "intrinsic" collector delay time $\tau_{CI}$ and "extrinsic" collector delay time $\tau_{CE}$. They are defined by

$$\tau_{CI} \equiv \left. \frac{\partial Q_{nCI}}{\partial I_C} \right|_{V_{CE} = \text{const.}} \tag{3}$$

$$\tau_{CE} \equiv \left. \frac{\partial Q_{nCE}}{\partial I_C} \right|_{V_{CE} = \text{const.}} \tag{4}$$

where $Q_{nCI}$ and $Q_{nCE}$ are electron charges in the intrinsic collector and extrinsic collector regions, respectively. $\tau_{CI} + \tau_{CE} = \tau_C$. $\tau_{CE}$ - $I_C$ and $\tau_{CI}$ - $I_C$ curves for $x_1 = 0$ are shown in Fig.6. It is seen that $\tau_{CE}$ decreases heavily by introducing the semi-insulating layer. This is because external base-collector capacitance decreases and so the charging time decreases. This contributes to improving $f_T$ in the low $I_C$ region. While, $\tau_{CI}$ increases in the high $I_C$ region by introducing the semi-insulating layer. This is because a high injection effect is enhanced by introducing the semi-insulating layer and the collector transit time increases, as de-

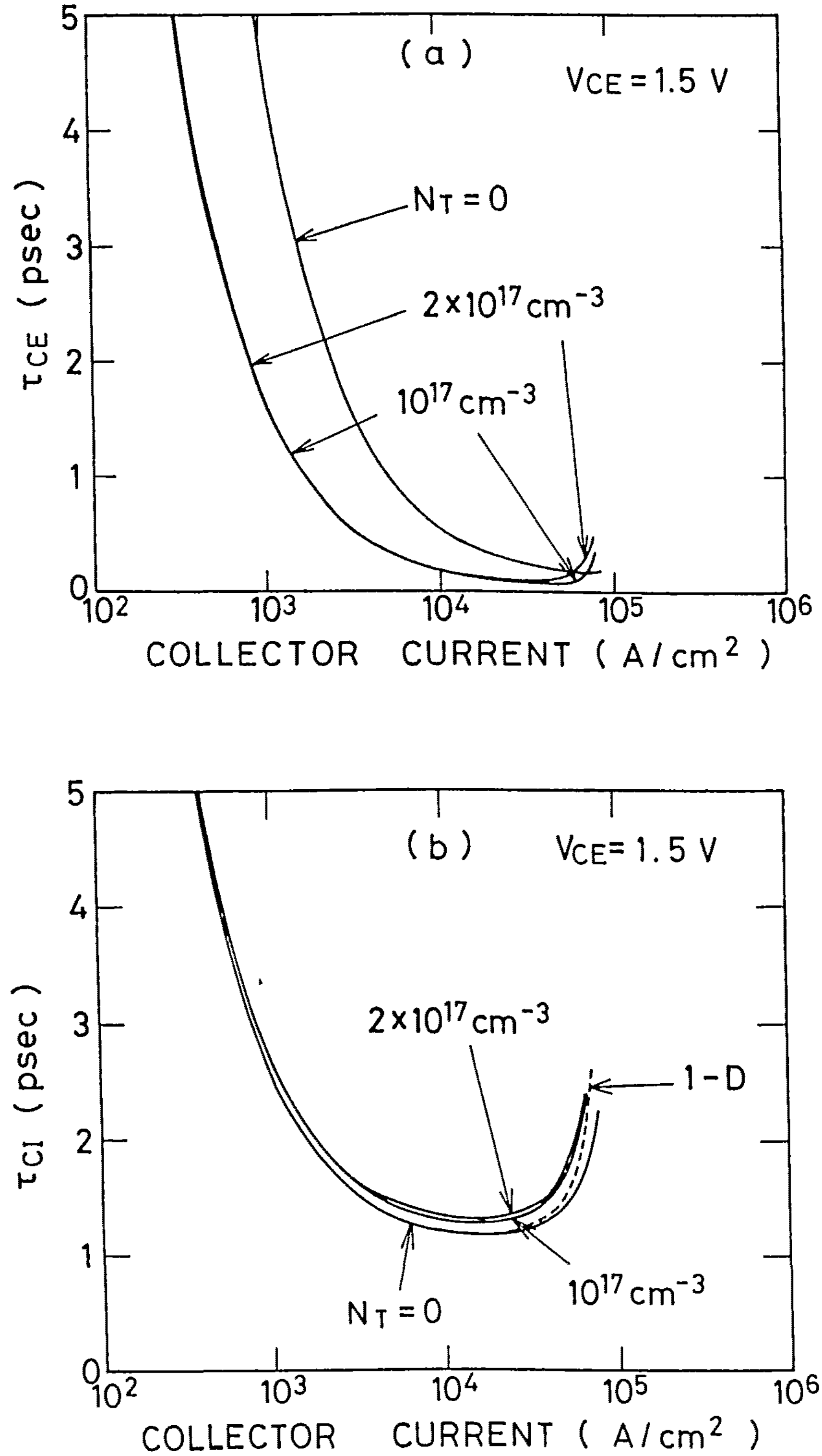


Fig.6 (a) Extrinsic collector delay time $\tau_{CE}$ and (b) Intrinsic collector delay time $\tau_{CI}$ as a function of $I_C$, corresponding to Fig.4 ($x_1 = 0$).

scribed below. Fig.7 shows a comparison of energy band diagrams of HBTs with and without a semi-insulating external collector. The collector current density normalized by emitter area is $6.5\times10^{4}$ $A/cm^{2}$ and it is a relatively high current level. In a case with a semi-insulating external collector, the expansion of collector depletion layer (near the $n^{-}$- i junction) is more remarkable, resulting in a longer transit time in this region. Therefore, $f_T$ falls earlier in the high current region.

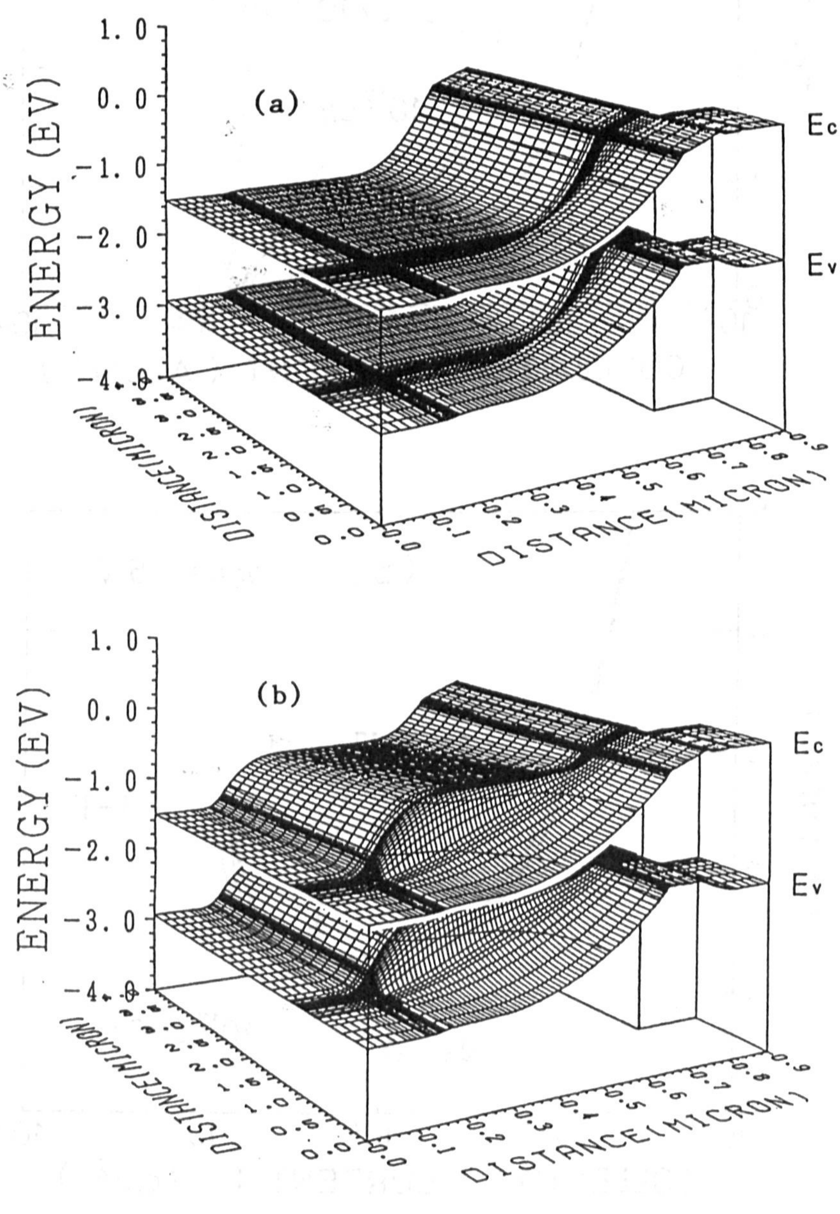


Fig.7 Comparison of energy band diagrams of HBTs with and without i-layer. $V_{CE}$ = 1.5 V and $I_C$ = $6.5\times10^{4}$ $A/cm^{2}$.
(a) Without i-layer, (b) With i-layer ($N_T$ = $10^{17}cm^{-3}$, $x_1$ = 0).

An easily interpreted way to reduce this unfavorable high injection effect (and to keep parasitic base-collector capacitance low) is to set the semi-insulating layer slightly away from the intrinsic collector region ($x_1 < 0$), as seen from Figs.4 and 5. By setting $x_1 < 0$, $f_T$ is improved in the whole $I_C$ region as compared to a case without a semi-insulating layer, as shown in Fig.4. When $|x_1|$ is too short, above high injection effect can't be so reduced. While, when $|x_1|$ is long, the parasitic base-collector capacitance becomes large. An appropriate value for $|x_1|$ depends on how far the space-charge layer at the $n^-$- i junction extends into the $n^-$-layer. The width of this layer is approximately given by $(2\varepsilon V_B/qN_{C1})^{1/2}$ where $V_B$ is the built-in potential. It becomes $\sim$ 0.13 μm in this case.

As described above, the introduction of semi-insulating external collector can lead to unexpected degradation of $f_T$ because of an enhanced high injection effect. Therefore, we must take care of this point. This phenonenon may be remarkable in small-sized devices.

## IV. Conclusion

Two-dimensional simulations of AlGaAs/GaAs HBTs with various collector structures are performed. It is shown that the transit time in collector depletion layer becomes a more important factor than the collector charging time in the high current region. Therefore, a thinner $n^-$-collector layer with higher doping density is desirable to achieve higher cutoff frequency. The introduction of semi-insulating external collectors is effective in improving cutoff frequency characteristics in relatively low current region, but it may lead to an earlier fall of $f_T$ due to an enhanced high injection effect. To reduce this unfavorable effect, the semi-insulating layer should be slightly away from the intrinsic collector so that it may not affect electron transport in the intrinsic collector region.

## References


1) P.M.Asbeck, M.F.Chang, J.A.Higgins, N.F.Sheng, G.J.Sullivan and K.-C.Wang, "GaAlAs/GaAs heterojunction bipolar transistors: Issues and prospects for application", IEEE Trans. Electron Devices, vol.36, pp.2032-2042, 1989.
2) T.Ishibashi and Y.Yamauchi, "A possible near-ballistic collection in an AlGaAs/GaAs HBT with a modified collector structure", IEEE Trans. Electron Devices, vol.35, pp.401-404, 1988.

3) P.M.Asbeck, D.L.Miller, R.J.Anderson and F.H.Eisen, "GaAs/(Ga,Al)As heterojunction bipolar transistors with buried oxgen-implanted isolation layers", IEEE Electron Device Lett., vol.EDL-5, pp.310-312, 1984.

4) O.Nakajima, K.Nagata, Y.Yamauchi, H.Itoh and T.Ishibashi, "High-performance AlGaAs/GaAs HBT's utilizing proton-implanted buried layers and highly doped base layers", IEEE Trans. Electron Devices, vol.ED-34, pp.2393-2398, 1987.

5) J.Yoshida, M.Kurata, K.Morizuka and A.Hojo, "Emitter-base bandgap grading effects on GaAlAs/GaAs heterojunction bipolar transistor characteristics", IEEE Trans. Electron Devices, vol.ED-32, pp.1714-1721, 1985.

6) A.Das and M.S.Lundstrom, "Numerical study of emitter-base junction design for AlGaAs/GaAs heterojunction bipolar transistors", IEEE Trans. Electron Devices, vol.35, pp.863-870, 1988.

7) P.I.Rockett, "Monte Carlo study of the influence of collector region velocity overshoot on the high-frequency performance of AlGaAs/GaAs heterojunction bipolar transistor", IEEE Trans. Electron Devices, vol.35, pp.1573-1579, 1988.

8) K.Horio, Y.Iwatsu and H.Yanai, "Numerical simulation of AlGaAs/GaAs heterojunction bipolar transistors with various collector parameters", IEEE Trans. Electron Devices, vol.36, pp.617-624, 1989.

9) Y.S.Hiraoka, J.Yoshida and M.Azuma, "Two-dimensional analysis of emitter-size effect on current gain for GaAlAs/GaAs HBT's", IEEE Trans. Electron Devices, vol.ED-34, pp.721-725, 1987.

10) M.Meyyappan, G.Andrews, H.L.Grubin and J.P.Krekovsky, "Analysis of a self-aligned AlGaAs/GaAs heterojunction bipolar transistor: Steady-state and transient simulations", J. Appl. Phys., vol.66, pp.3348-3354, 1989.

11) S.Tiwari and D.J.Frank, "Analysis of the operation of GaAlAs/GaAs HBT's", IEEE Trans. Electron Devices, vol.36, pp.2105-2121, 1989.

12) K.Horio, K.Asada and H.Yanai, "Two-dimensional simulations of GaAs MESFETs with deep acceptors in the semi-insulating substrate", Solid-State Electron., vol.34, pp.335-343, 1991.

13) T.Shawki, G.Salmer and O.El-Sayed, "MODFET 2-D hydrodynamic energy modeling: Optimization of suquarter-micron-gate structures", IEEE Trans. Electron Devices, vol.37, pp.21-30, 1990.

14) K.Horio, Y.Fuseya, H.Kusuki and H.Yanai, "Small-signal parameters of GaAs MESFET's as affected by substrate properties — Computer simulation —", IEICE Trans., vol.E74, no.5, 1991.