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Electrical and Thermal Analysis of VLSI Contacts and Vias

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Summary

Numerically simulated temperature distributions in fine geometry contacts and vias are presented for realistic physical/material parameters and operating conditions. Due to the relatively low interfacial electrical conductivity in the contact geometry, large electric potential gradients develop, consequently leading to high Joule heating effects. In the case of the via, temperature escalations result from singularities in the electric field at geometrically imperfect locations due to inadequate step coverage in the metallisation process. Details of the numerical procedure, in particular, the boundary conditions for the temperature equation are discussed.

Introduction

With the continuing reduction in feature size of integrated circuits, long term reliability is a growing concern. Besides the failure mechanisms at the device level, several other effects that could previously be ignored, are now becoming crucial with respect to reliability. Such effects are [1]: metal penetration depths and contact depths that are a significant fraction of a shallow junction, inadequate step coverage associated with reduced contact and via areas, the increased current density in the fine geometries, and the high contact resistance leading to degradation of electrical performance. The high current densities in (Al/Si) metallisation interconnects, contacts, and vias

result in temperature escalations and promote electromigration-induced failures.

Electromigration induced damage takes place with the formation of voids and hillocks on the metallisation geometries. Voids ultimately result in discontinuities in the conductor and hillocks can lead to short circuiting effects with adjacent metallisation regions. The atomic flux j due to migration is a function of the electric current density J flowing through the conductor and the temperature T [1], viz.,

$$j \propto J \rho (qZ^*/kT) D_0 e^{-Q/kT}, \tag{1}$$

where ρ is resistivity of the conductor, qZ^* the effective charge, D_0 the grain boundary diffusion coefficient, and Q is diffusion activation energy.

In this paper, we present two-dimensional numerical results for temperature distributions in fine geometry contacts and vias. The results have been obtained for realistic material parameters. Typically, these structures are circular (see Fig. 1). For purposes of a two-dimensional simulation, we have introduced an artificial region which assumes a lumped value of electrical conductivity to account for the current flow in the z-direction (see shaded area in Fig. 1b). The interface resistance for the contact or via is accounted for by defining a "transition region" of thickness 750 Å whose conductivity would yield the measured values of contact or via resistance. Knowledge of the electric field (and consequently the current density) as well as temperature distributions, can be used to optimise the geometry (e.g. aspect ratio) of these structures. This may even lead to the choice of new materials in order to to minimise failures induced by electromigration.

Model Equations and Boundary Conditions

To obtain estimates of contact resistance in VLSI contacts, contact chain or cross bridge Kelvin type measurement arrangements are generally employed. For either configuration at low current operation, it is reasonable to assume that the flow of current in the N+ region (source or drain diffusions) is confined to within a narrow region (~ 0.6 x_j) beneath the oxide semiconductor interface. With selected dopants, this region can be considered as homogeneously doped and the minority

carrier current as well as the recombination can be assumed negligible. Under these conditions, the equations governing the electrothermal behaviour in a (Al/Si) - N+ Si contact can be reduced to

$$\text{div}\ [\sigma_n(T)\ \text{grad}\ \psi] = 0 \tag{2}$$

$$\text{div}\ [\kappa(T)\ \text{grad}\ T] = -\ \sigma_n(T)\ (\text{grad}\ \psi)^2, \tag{3}$$

where $\sigma_n(T)$ and $\kappa(T)$ denote the temperature dependent electrical and thermal conductivities, respectively. These parameters account for changes in the electrical and thermal properties in the different materials. Although it is not common practice to solve eqn. (1) for the electrical potential, we have opted for this procedure since it takes into account parameters whose values have been experimentally determined. Following the standard route of solving the usual Poisson's equation for the electric potential would require the assumption of an appropriate interface charge. In addition, the actual value of the permittivity of the metallisation material (Al/Si) is not known.

Equations (2) and (3) with realistic values of the various parameters, are solved subject to Dirichlet, homogeneous Neumann, and mixed boundary conditions. At the contact regions, standard Dirichlet conditions are assumed for the electric potential, i.e. ψ is prescribed by the applied voltage. At metal/insulator interfaces, we assume that the interfaces are ideal (zero surface recombination) and hence the normal component of current density at these boundaries is forced to be zero: $\boldsymbol{E} \cdot \boldsymbol{n} = 0$ ($\boldsymbol{n}$ here denotes the outward normal vector). At interfaces between two different electrically conducting media, the condition of electric current continuity

$$\sigma_1\ (\boldsymbol{E} \cdot \boldsymbol{n})_1 = \sigma_2\ (\boldsymbol{E} \cdot \boldsymbol{n})_2 \tag{4}$$

is imposed. This condition occurs naturally in the weak formulation of the equations. We observe that eqns. (2) and (4) inherently account for interface charge.

The boundary conditions for the temperature are most important in this problem. The side boundaries ($x = 0$ and $x = 5.2$ µm; see Fig. 1) of the simulation domain are assumed adiabatic. At the top of the simulation domain ($y = 5$ µm), we assume either an adiabatic or a

Dirichlet condition. The former condition is necessary with flip chip mounting and the latter simulates a situation where the top surface of the chip is maintained at an ambient temperature of 300 °K. For the bottom face of the simulation domain ($y = 0$), a mixed boundary condition is employed. In cases of backside mounting, the heat sink is typically 300 μm below the active chip area, where all the heat sources and sinks are distributed. Simulating the thermal behaviour for the entire wafer thickness can be computationally intensive. Consequently, we have selected the following procedure. Equation (3) for the bulk becomes

$$\text{div}\ (\kappa_s\ \text{grad}\ T) = 0 \tag{5}$$

with κ_s denoting the thermal conductivity of bulk Si. As a first approximation, κ_s is assumed to be temperature independent. In view of the spatial symmetry of the problem, it is reasonable to assume that in the bulk, the direction of heat flux is normal to the bottom boundary. If the temperature there ($y = 0$) is T, and the heat sink temperature at the wafer backside ($d \approx 300$ μm) is T_0, the continuity of heat current at the $y = 0$ plane leads to

$$\kappa(T)\ (\text{grad}\ T\ .\ \boldsymbol{n}) = \kappa_s\ (T_0 - T)/d, \tag{6}$$

where $\boldsymbol{n}$ is the normal vector pointing towards the wafer backside and $\kappa(T)$ denotes the thermal conductivity of the material in the vicinity of $y \geq 0$. Note that relation (5) is consistent with the weak formulation of the equations. This condition gives an indication of the numerical difficulties involved in this problem. If $d = \infty$, then the $y = 0$ boundary becomes adiabatic and the resulting problem is singular (since the other edges have been assumed adiabatic as well). On the other hand, if $d = 0$, the $y = 0$ boundary is fixed at $T = T_0$ and the problem is stable.

Although eqns. (2) and (3) appear to be in a similar form, the role of the boundary conditions are remarkably different for the two quantities, ψ and T. This is a consequence of the physical character of these quantities.

The dependence of the electrical conductivity on temperature in the N+ region is taken into account *via* the temperature dependent intrinsic concentration and the drift mobility. Here, the Fermi potential of the

electrons is assumed uniform and pinned to the applied voltage at this region. The dependence of the drift mobility on temperature is assumed to follow the model proposed by Aurora et al. (see [2]). The thermal conductivity in this region is assumed to obey the model

$$\kappa(T) = (a + bT + cT^2)^{-1} \tag{7}$$

proposed by Glassbrenner and Slack (see [2]). The values of the various coefficients can be found in [2]. In the contact region, σ is assumed to be independent of temperature and a value consistent with experimental estimates of contact resistance is adopted. The thermal conductivity in this region is taken to be temperature independent and identical to that of the N+ Si. In the metallisation regions, σ is proportional to $(1/T)$ with its value at ambient temperature as measured. On the other hand, κ is independent of T and is assumed to be 2.37 W/cm°K. For the artificial region (shaded in Fig. 1b), σ assumes a lumped value accounting for current flow in the z-direction, while κ in this region is that of the oxide. The values of κ employed in the oxide regions can be found in [3].

Numerical Procedure

The model equations described above are discretised on an adaptively generated triangular grid. A fine mesh is employed at the interfaces between the different regions where significant changes in the material parameters, particularly in the electrical conductivity occur (see Fig. 2). The discretisation scheme is based on the box integration method [4], which we have extensively used in our previous work [5]. The present problem required extensions of the existing code to take into account the additional physical parameters as well as the mixed boundary condition. The solution process is based on a linear procedure using a successive scheme. The potential equation is first solved with the temperature set to the ambient value, followed by the solution process of the weakly nonlinear temperature equation. The solution to the potential equation is restricted to within the conductive regions, while the temperature equation is solved over the entire domain. The values of the pertinent parameters are updated each time the iteration loop is completed. The system is iterated until self-consistent values of ψ and T are achieved. Due to the nature of the system (linear potential equation and weakly nonlinear temperature equation), we did not experience

convergence difficulties even at large operating currents (and hence large temperatures).

Results and Discussion

The maximum temperature, T_{max} in the contact domain was investigated for various wafer thicknesses, d with the wafer backside maintained at an ambient temperature, $T_0 = 300$ °K (see Fig. 3). For the top and side boundaries, we imposed an adiabatic condition. As expected, T_{max} as well as the minimum temperature, T_{min} decrease with diminishing wafer thickness. T_{max} appears at $x = 1.55$ µm, $y = 1.9$ µm, and T_{min} at $y = 0$. Replacing the boundary condition at $y = 0$ with a Dirichlet condition ($T = T_0$) yields a maximum temperature of 358 °K, which confirms the trend observed by extrapolating T_{max} on Fig. 3 to $d = 0$. As the heat sink becomes more remote (increasing wafer thickness d), the ratio T_{max}/T_{min} decreases and finally reaches the value 1. For diminishing wafer thickness, T_{max}/T_{min} increases and approaches a constant value larger than 1. This suggests that use of smaller wafer thickness could reduce high temperarture-induced failures.

Isothermal lines are shown in Fig. 4 for the contact with the mixed boundary condition at $y = 0$, the temperature fixed at T_0 at the top, and adiabatic side boundaries. We note that majority of the heat is generated in the contact resistance region. Due to the relatively high interfacial resistance, the electric fields in this region are large (and so is the localised electric current density), consequently resulting in high Joule heat. The maximum temperature observed under these conditions is 791 °K at $x = 1.55$ µm, $y = 1.9$ µm, which happens to be the left corner of the contact resistance region where singularities in the electric field occur.

In the case of the via (Fig. 5), the temperature escalations are solely due to geometrical effects. When stressed with a current density of 2.63×10^6 A/cm^2, a hot spot of 17°K above the ambient temperature develops at $x = 1.55$ µm and $y = 3$ µm. At this location, due to the inadequate step coverage of the metallisation process, relatively large potential gradients develop at the corners resulting in current crowding effects. These are potential locations for electromigration-induced failures. In particular, at such locations, depending on the processing conditions, cracks in the

(Al/Si) thin film may result. This gives rise to singularities in the electric field (and consequently the electric current density), leading to significant escalations of the temperature.

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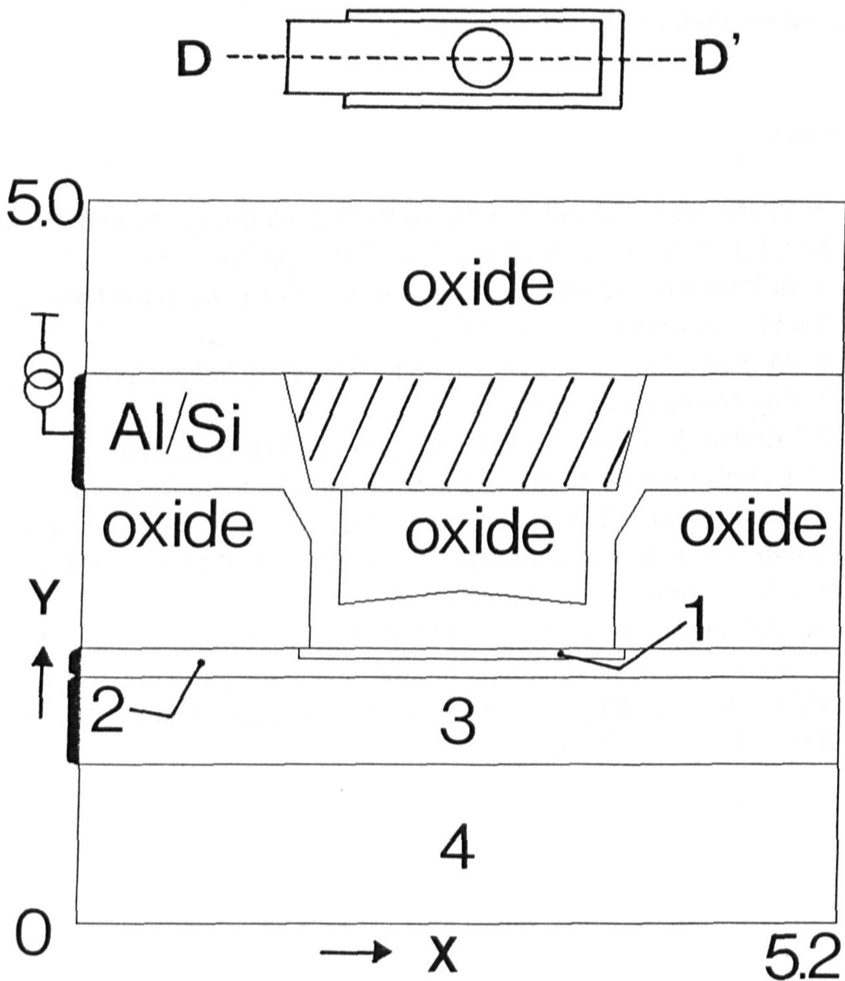

Fig. 1. (a) Top view of a contact or via.
(b) Simulation domain (DD') of contact or via. Shaded region accounts for effective current flow in *z*-direction.
For a contact, **1**: contact resistance region, **2**: N+ Si, and **3**,**4**: bulk Si. The lower electrode is only at **2**.
For a via, **1**: via resistance region, **2**,**3**: (Al/Si), and **4**: oxide. The lower electrode is in **2** and **3**.
(The figure is drawn to scale and dimensions are in μm)

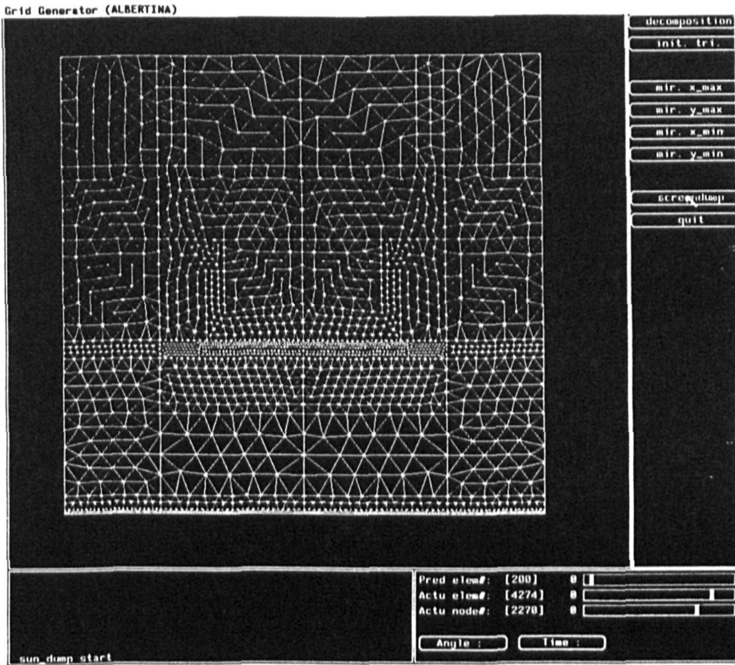

Fig. 2. Mesh used in simulations.

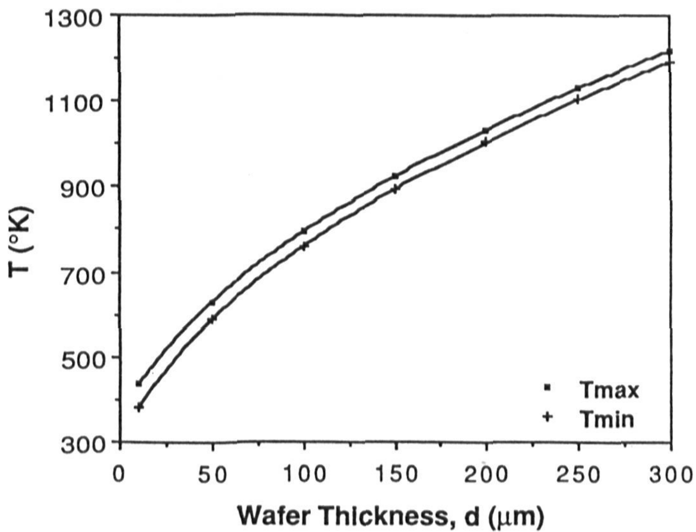

Fig. 3. The maximum and minimum temperatures in the domain as a function of wafer thickness.

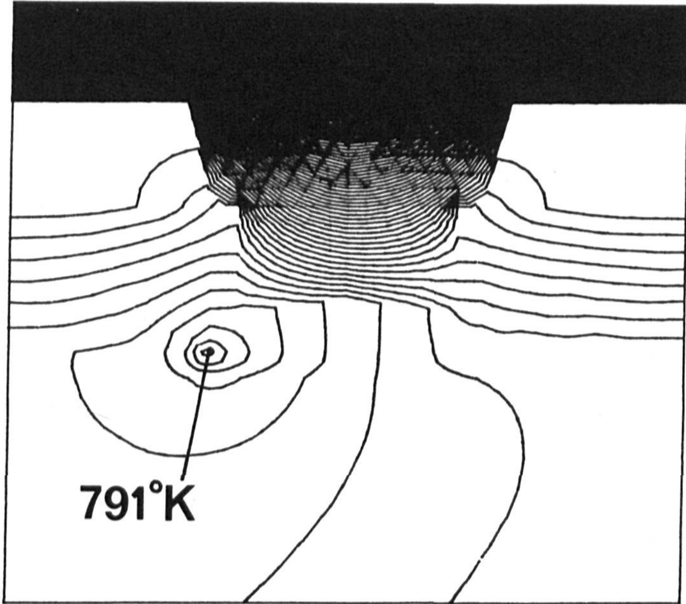

Fig. 4. Isothermal lines in the contact with $R_C = 65\ \Omega$ and $I = 1$ mA. Contact diameter is 1.9 μm. Top boundary is at 300°K.

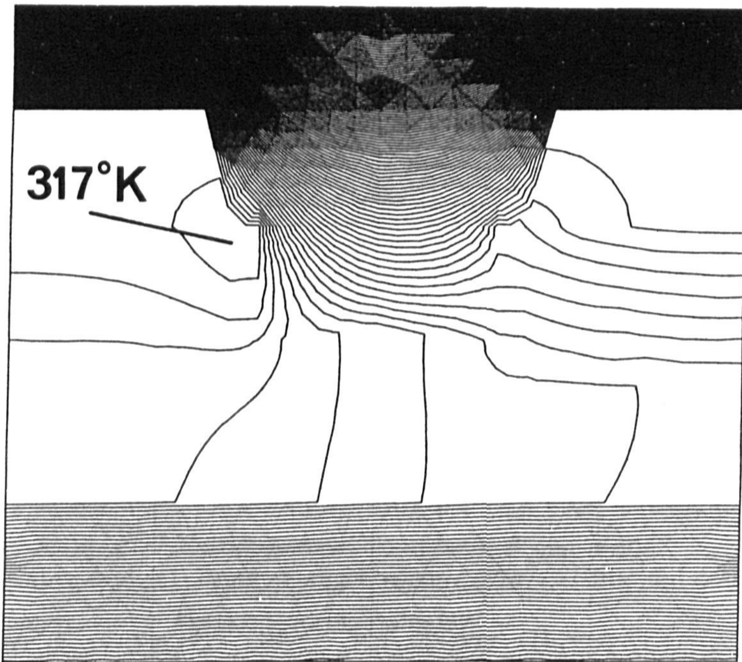

Fig. 5. Isothermal lines in a via with $R_{via} = 120\ \text{m}\Omega$ and $J = 2.63 \times 10^6\ \text{A/cm}^2$. Top boundary is at 300°K.