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NUMERICAL SIMULATION OF TRANSIENT AND HIGH FREQUENCY PERFORMANCE FOR SUBMICRON CMOS AND SOI/CMOS GATE AND RING OSCILLATOR

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SUMMARY

The novel two-dimensional simulators for submicron CMOS and SOI/CMOS gate and ring oscillator are developed using a numerical scheme of alternating direction method and alternative step method to provide rapid convergency and high accuracy. The simulators, combining device simulation and circuit simulation, can be used to reveal physical insight in device and predict circuit transient and high frequency performance. Coupling effect of load and inverter is first considered. Voltage waveforms of CMOS and SOI/CMOS ring oscillators has also been simulated successfully.

INTRODUCTION

The Total Quantity of Carrier method (C.Huang, 1986) was used in this work to inverstigate the transient behaviour of device with emphasis on build up and decay of carriers to provide clear physical insight. Although many papers have been published for device simulation (K.yamaguchi, 1983. M.Tomizawa, 1982), they can not provide realistic transient characteristics for a submicon CMOS gate, especially for SOI/CMOS gate with evident floating body effect. For SOI/CMOS, impact ionization and recombination mechanism are considered in transient transport equation because the substrate is floating. In a CMOS inverter circuit, the output voltage is time-dependent and changes with the magnitude of channel currents of the load an drive device to charge or discharge the capacitive load. In order to provide more accurate device design tool, the simulators, combining device simulation

and circuit simulation with a capacitive load. have been developed with an efficient numerical scheme. These two-dimensional simulators, LADES-2A(Lishan Advance DEvice Simulabtor, version 2A) for bulk CMOS gate and LADES-4G for SOI/CMOS gate, have been used to explore transient and high frequency behavior of carrier distribution, electric potential, as well as circuit output performance .

NUMERICAL SCHEME

The numerical model includes Poisson's equation and two-carrier continuity equation, that is

(1) $$\nabla^2\phi = -\frac{q}{\varepsilon}(p - n + N_D - N_A)$$

(2) $$\frac{\partial n}{\partial t} = \nabla \cdot (-n\mu_n\nabla\phi + D_n\nabla_n) + G - R$$

(3) $$\frac{\partial p}{\partial t} = -\nabla \cdot (-p\mu_p\nabla\phi - D_p\nabla p) + G - R$$

Here, the variables , n, p denote the electrical potential, electron and hole densities, respectively. Jn and Jp include the drift and diffusion terms,

(4) $$\mathbf{j}_n = -n\mu_n\nabla\phi + D_n\nabla \mathbf{n}$$

(5) $$\mathbf{j}_p = -p\mu_p\nabla\phi - D_p\nabla p$$

For SOI devices , the generation and recombination mechanism must be included in the continuity equations because there is accumulation of minority carrier produced by impact ionization which causes the device to have anomalous steady state and transient state characteristics. Generation and recombination terms in continuity equations include three basic processes: Avalanche generation due to impact ionization, Auger recombination due to transition through a bandgap, and thermal generation and recombination via trap level. These processes are modeled by the following expressions:

(6) $$(G\text{-}R)\ \text{avalanche} = \left[A_n|J_n|\exp\left(-\frac{B_n}{|\nabla\phi|}\right) + A_p|J_p|\exp\left(-\frac{B_p}{|\nabla\phi|}\right)\right]$$

(7) $$(G\text{-}R)\ \text{Auger} = (np - n_i^2)(C_n n + C_p p)$$

(8) $$(G\text{-}R)_{thermal} = \frac{np - n_i^2}{(n + n_i)\tau_p + (p + n_i)\tau_n}$$

Where the parameters in equation (6)-(8) are given in paper (S.P.Gaur, 1985).

A new algorithm, alternating direction scheme (S.Xiao, 1987) is used for solving transient continuity equation. The main idea of alternating direction scheme is that for time step $\Delta t(2m+1)$, the differential terms in x iterated implicitly, while the terms in y direction are kept the values of time step $\Delta t(2m)$, and for the time setp $\Delta t(2m+2)$, the procedure is just opposite to that of $\Delta t(2m+1)$. The two procedures are carried out alternately on successive time steps of Δt each, which can been written as:

(9) $$(n_{i,j}^{2m+1} - n_{i,j}^{2m})/\Delta t = (J_{i+\frac{1}{2},j} - J_{i-\frac{1}{2},j})^{2m+1}/hx + (J_{i,j+\frac{1}{2}} - J_{i,j-\frac{1}{2}})^{2m}/hy + (G - R)^{2m}$$

(10) $$(n_{i,j}^{2m+2} - n_{i,j}^{2m+1})/\Delta t = (J_{i+\frac{1}{2},j} - J_{i-\frac{1}{2},j})^{2m+1}/hx + (J_{i,j+\frac{1}{2}} - J_{i,j-\frac{1}{2}})^{2m+2}/hy + (G - R)^{2m+1}$$

Where $J_{i,j}$ is the current density at mash point(i, j).

This scheme has been proved to be more efficient than conventional C-N scheme in following aspects:

(1) The new scheme converts the two-dimensional equation into two successive one dimensional equations, thus reducing calculating time significantly.

(2) With fast convergency for bulk CMOS devices, the number of cycle for internal iteration is about 60% less than that of C-N scheme.

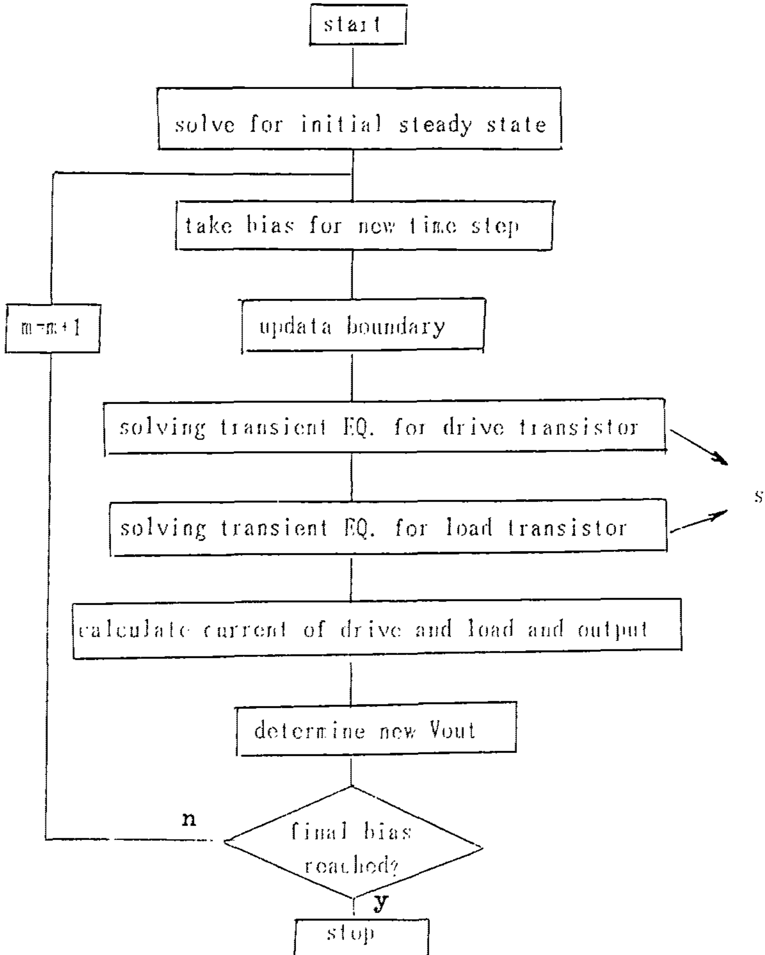
(3) satisfying the same stability for time-dependent equations, larger time step is allowed.

However, avalanche generation due to impact ionization in SOI device is very sensitive to electric field and current density, the simultaneous solution of Poisson's equation and continuity equations even by alternating direction method may not converge when impact ionization becomes significantly (M.Du, 1988). For SOI/CMOS, the calcublation of transport equations is devided as an outer loop consisting of three equations and an inner loop of strongest coupling equations (Poisson's and electron continuity equations for n-channel device). If numerical error is too large by impact ionization effect, the inner loop begins. After the inner loop converges, the outer loop begins.

Boundary conditions of CMOS inverter for the transport equations are assumed as follows. At source, drain, and gate, electrical potential is determined by applied voltages. In transient circuit, Vout is time-dependent with the drive and load devices to charge or discharge the capacitive load. That is

(11) Vout(t+ t)=Vout(t)+(I (t)-I (t))dt/Cout

Where Cout is a capacitive load. I (t) and I (t) are transient drain currents of the load and drive device. The normal components of electric displacement D at gate-oxide-Si and Si-backgate-oxide interfaces are continuous. A simple flowchart for solving a set of partial differential equations and the calculation of the gate transient response is illustrated in Fig.1.



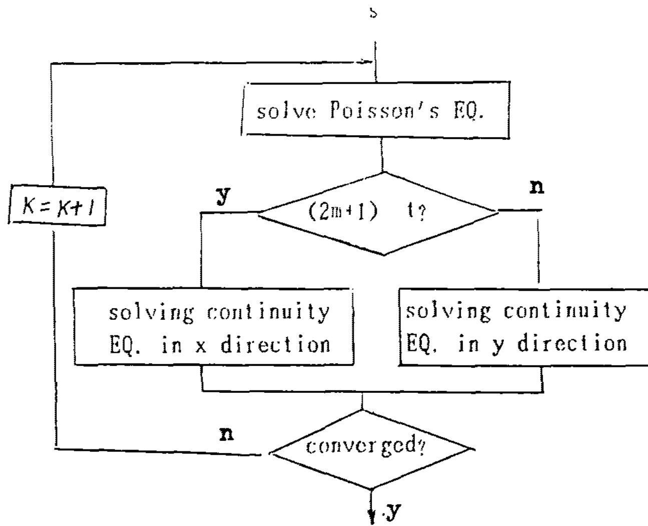


Fig.1 The general flowchart of the program

RESULTS AND DISCISSIONS

The transient numerical simulation for bulk and SOI CMOS inverter has been developed based on the description in the previous section. Using the symmetry property, waveform of CMOS ring oscillator has also been simulated by trial function scheme (H.Tian, 1988). High frequency performance of MOSFET is first simulated by applying a high frequency sine wave signal to the gate. Here we show some examples for its validity and advantage.

(1) CMOS inverter structure

Unlike that in a signel device, the build up of total channel carrier in NMOSFET not only depends on the input pulse, but also on the decay of channel carriers in PMOSFET and on the output capacitive load. Output voltage and current response of a CMOS inverter is shown in Fig.2, with a ramp input of 0-3v in 0.1ns. Dashed line presents the result obtained by equating current of drive and load transistors based on assumption in (M.Tomizawa, others, 1982). As a matter of fact, the transient performance of inverter in practical application not only depends on its own driving capability, but also has close relation with parastic and load capacitance. From the result, we can see that only when capacitance charging or discharing effect is . taken into consideration, will it be possible to get realistic and reasonable prediction of circuit transient performance.

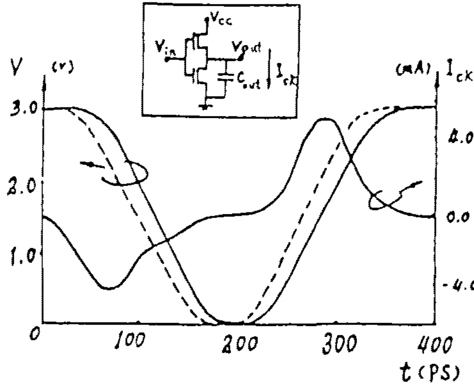


Fig.2 output voltage and charging or discharging current response of CMOS inverter. Dashed line is the result by neglecting output capacitive load. L=1μm, Wn=10μm, Wp=30μm, Cout=0.1pf Vcc=3.0v

(2)SOI/COMS transient analysis

The unique behaviors of submicron SOI divice in CMOS inverter have been simulated by LADES-4G. The physical picture of floating body effect is presented. When a SOI/CMOS inverter changes state from off to on, the floating substrate will result in drain current overshoot for the n-channel devive because the long lifetime of excess holes. Fig.3(a) and Fig.3(b) show the two-dimensional distribution of generation rate and recombination rate in a n-channel device at time=20 ps, Vin=1v, Vout=3v. There is a sharp peak near substrate-drain junction in Fig.3(a) and a peak of recombination in source-substrate region in Fig.3(b). This behavior can be explained as follows. For the SOI device, excess holes are surrounded by n+ regions and insulator layer, they have no way to escape unless by recombination process. If a short channel MOSFET operates in high drain-source bias, electron-hole pairs are generated by impact ionization as moving carriers pass through the drain region where the electric field is strong. The excess holes move towards source under the effect of the field to recombine with electrons injected from the source. It should be noted that floating body effects in a inverter not only depend on recombination mechanism of minority carrires accumulated in the floating body, but also vary with the time-dependent input and output voltages. Fig.4(a) and Fig.4(b) give the distributions of generation rate and recombination rate at time=80ps, Vin=2v, Vout=1v. It is clear that generation rate decreases with decreasing of drain voltage. Comparing Fig.3(b) and Fig.4(b), the peak value of recombination rate near source-substrate region becomes higher as gate bias increases.

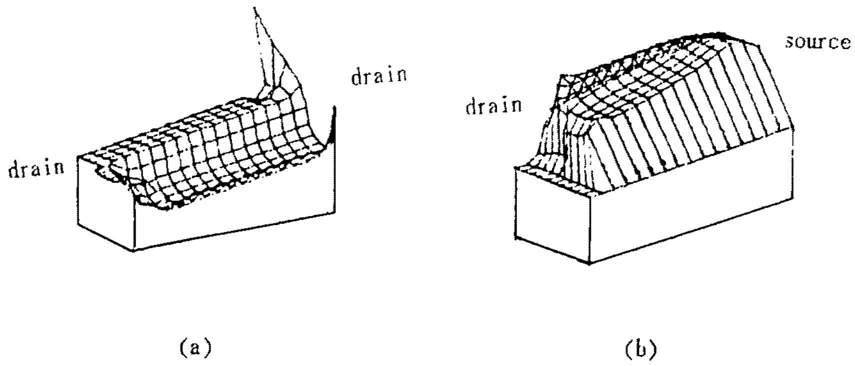


Fig.3 Generation rate and recombination rate distributions. time=20ps, vin=1v, vout=3v L=0.5μm, Na=1.e17cm-3

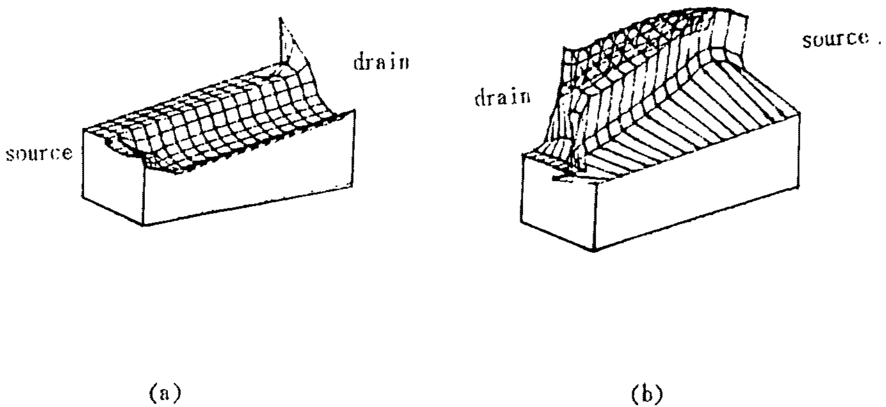


Fig.4 Generation rate and recombination rate distributions. time=80ps, vin=2v, vout=1v L=0.5μm, Na=1.e17cm-3

Therefore, floating body potential can have various values which depend on bias conditions and generation-recombination mechanism. The floating substrate effect increases drain current and improves SOI CMOS speed.

(3) Ring oscillator and high frequency simulation

Ring oscillator is simulated by varying the trial function of input voltage until it matches the output waveform with a stage delay between input and output nodes. The circuit is fabricated with implanted-buried oxide silicon film. In order to reduce hot carrier effect, n-channel device is designed as LDD structure with spacers 150 nm, the p-channel MOSFET is designed to be in the deep depletion mode with boron implant dose of 5×10^{11} cm-2 at 150 kev. Fig.5 is the per stage delay time versus channel length for the ring oscillator.

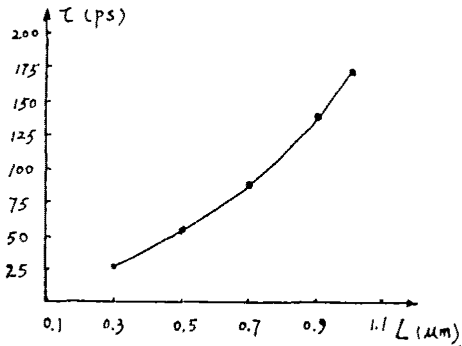


Fig.5 Simulated results of per stage deley time of a ring oscillator fabricated with implated-buried-oxide silicon film.
Vcc=5v, Tsi=0.2μm, Wn=10μm, Wp=20μm

High frequency performance of MOSFET is first simulated by numerical method by applying a high frequency sine wave signal to the gate. Simulated device transconductance dependence on operating frequency is show in Fig.6. It is verified in this work the main reason that degrades device high frequency operation is not carrier transient time across channel, but build up and decay of channel carriers.

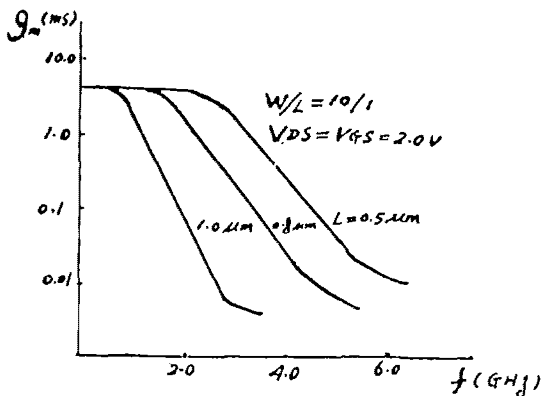


Fig.6. Transconductance dependence of frequency for NMOSFET

CONCLUSION

The new simulators LADES-2A and LADES-4G have been developed using numerical scheme of alternating direction method and alternative step method to provide rapid convergency and high accuracy for transient and high frequency simulation of gate level CMOS and SOI/CMOS devices. The transient and high frequency numerical analysis have been carried out using the two-carriers and two-dimensional simulators. The set of simulators can be used for optimization of CMOS and SOI/CMOS gate device design as well as more accurate equivalent circuit development and parameter extraction.

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