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SITAR - An Efficient 3 D-Simulator for Optimization of Non-planar Trench Structures

W. Bergner and R. Kircher,
SIEMENS AG, Corporate Research and Development,
Otto-Hahn-Ring 6, 8000 München, West-Germany

SUMMARY

A 3-dimensional device simulator is presented which allows the investigation of the electrical behaviour of non-planar trench-type device structures. It has been used to analyze leakage due to punch through between neighbouring trench capacitors, depending on geometry and doping profiles. By its completely vectorized solution algorithm it proved to be a very efficient tool to optimize the cell size of 4 Megabit DRAMs.

INTRODUCTION

With increasing packing density the geometrical size of the single device structure becomes smaller and smaller. For the 4 Megabit DRAM the minimum feature size is 0.5 µm. However, some structures, especially storage capacitors, need a minimum area to maintain safe circuit operation. In VLSI dynamic memories the storage capacitor is extended into the bulk material as a so-called trench capacitor, leading to a 3-dimensional behaviour with parasitic effects, e. g. leakage current due to punch through. To optimize the geometry parameters of such a cell structure for use in modern 4 Megabit or 16 Megabit DRAMs, one has to include all effects arising from the 3-dimensional geometry, especially for non-uniform doping distributions. The 3-dimensional device simulator SITAR (SIemens Trench AnalyzeR) has been developed to investigate the electrical behaviour of non-planar trench-type cell structures, depending on geometry, doping profiles and applied voltages. In this paper SITAR has been used to optimize the leakage behaviour of 4 Megabit DRAMs due to punch through between neighbouring trench capacitors.

THE SIMULATOR

The device simulator SITAR solves the phenomenological semiconductor equations

$$\nabla\cdot\varepsilon\nabla\Psi = -q\,(p - n + N_D^+ - N_A^-) \tag{1}$$

$$\begin{aligned}\nabla\cdot\vec{j}_n &= G - R\\ \nabla\cdot\vec{j}_p &= G - R\end{aligned} \tag{2}$$

with

$$\begin{aligned}\vec{j}_n &= \mu_n\left(n\nabla\Psi - \frac{kT}{q}\nabla n\right)\\ \vec{j}_p &= -\mu_p\left(p\nabla\Psi + \frac{kT}{q}\nabla p\right)\end{aligned} \tag{3}$$

in steady state and in 3 dimensions by using the finite difference method, where Ψ is the electrostatic potential, p and n the carrier densities, and $\vec{j}_n$ and $\vec{j}_p$ the corresponding current densities.

The finite difference mesh has to be defined by the user and is kept fixed during the simulation. By introducing a box integration algorithm for the current continuity equations it becomes possible to treat general non-planar interfaces between the silicon area and different dielectric materials. Special routines for the discretization guarantee an accurate resolution of non-planar interfaces.

The number as well as the combination of the equations to be solved in a Gummel's cycle can be chosen. The stopping criterion for the corrections in the linear and in the non-linear equations can be specified by the user. To find an efficient solution method for the inversion of the very large sparse matrix poses a rather complicated problem. For the simulations presented in this paper we have chosen a SOR-technique. The advantage of this algorithm is the high vectorization rate, which is almost 100 % in the presently implemented solver. In contrast to the vectorization is the rather slow convergence, especially for non-symmetric matrices, e. g. the discretized continuity equations.

Under various boundary conditions implemented in SITAR are Dirichlet conditions for ohmic and gate contacts, and Neumann conditions for artificial boundaries, e. g. device boundaries. Thin gate oxides can be treated analytically by a formula for an 1-dimensional MOS capacitor.

The 3-dimensional doping distribution can be defined either by a user-written subroutine or taken from 1D or 2D process simulations together with a suitable extension into the other dimensions. For trench-type structures a universal parameterization for the geometry and the doping profiles has been developed.

The physical models implemented in SITAR include scattering on ionized impurities, lattice and carriers [1]. In the mobility of electrons and holes, saturation of the field dependent velocity [2] is taken into account. High doping effects are included via band gap narrowing [3]. The generation/recombination model contains the mechanism of Shockley, Read and Hall and the Auger-effect. Impact ionization is not included in the generation model, but the ionization integral can be estimated by a post-processing calculation to find the breakdown voltage at reverse biased pn-junctions.

To minimize the computational effort for the trench cell optimization an analytical solution of the 1-dimensional continuity equation has been derived. For the case of punch through currents an expression similar to the subthreshold current of a MOSFET is obtained [4].

$$I_{pt} = q \cdot n_i \cdot \mu_n [A_{eff}/L_{eff}] \exp(q\Psi_o/kT), \tag{4}$$

where L_{eff} is the effective length and A_{eff} the effective cross section of the leakage channel at the saddle point $\vec{r}_0$ of the potential distribution between neighbouring trenches, n_i and μ_n are the intrinsic carrier density and the electron mobility, respectively [4]. The parameters Ψ_o, L_{eff} and A_{eff} can be determined by the 3-dimensional solution of Poisson's equation.

$$\Psi_o = \Psi(\vec{r}_o) \tag{5}$$

$$L_{eff} = \int_{\text{trench 1}}^{\text{trench 2}} \exp\{q(\Psi_o-\Psi)/kT\}\, dx \tag{6}$$

$$A_{eff} = \int_{\text{cross sect.}} \exp\{q(\Psi-\Psi_o)/kT\}\, dydz \tag{7}$$

Selecting this analytical model, the terminal currents are estimated as a function of the applied voltages, and the computational effort for the calculation of the I-V characteristic by the full 3-dimensional equations can be reduced drastically. The current values calculated by the analytical model and the 3-dimensional continuity equations agree within one order of magnitude.

TRENCH CELL OPTIMIZATION

For recently developed 4 and 16 Megabit DRAMs trench capacitors are used which provide enough capacitance at high integration density. However, integration density and variations in technology may result in leakage due to punch through between 2 neighbouring trench capacitors. The device simulator SITAR has been used to investigate punch through between neighbouring trench capacitors depending on geometry and doping profiles, and to optimize the isolation behaviour of 4 Megabit DRAMs. A typical structure used in the simulation is shown in Fig. 1. The parameters of the geometry of the

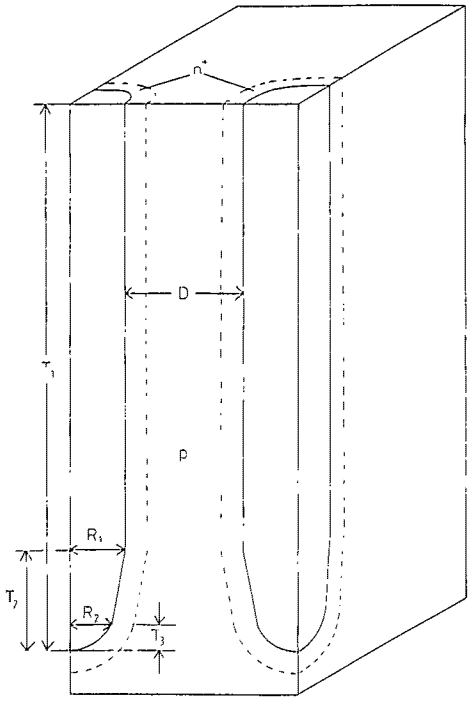

Fig. 1: Geometry of the simulated trench capacitor cell. The parameters are to be defined in the input file.

trenches are read in from the input file together with the parameters of the doping profile. The qualitative shape of the calculated I-V characteristic is shown in Fig. 2. It exhibits

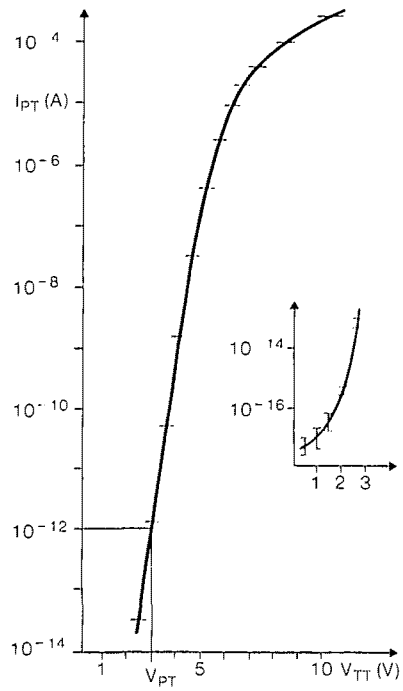

Fig. 2: Trench to trench leakage current as a function of the applied voltage.

a transition from generation currents at small reverse bias to the exponentially increasing subthreshold region at higher trench-trench bias. For very high bias conditions a transition to the linear region can be seen.

To get a physical insight into the influence of 3-dimensional effects on punch through, the trench to trench leakage current has been calculated for homogeneously doped substrate and different trench geometries as a function of trench to trench distance and impurity concentration. By assuming a critical leakage current of 1pA, based on the sensitivity of the amplifier circuit, the punch through voltage V_{pt} can be extracted, as indicated in Fig. 2. Renormalizing the effective trench to trench distance by the Debye length, we found an universal dependence of V_{pt} on the normalized distance for homogeneously doped substrate. Fig. 3 shows the result for 2 trench geometries compared with a simple analytical solution (dashed line) for abrupt npn-junctions along the cross section through the structure in Fig. 1 in depletion approximation. The punch through voltage is strongly influenced by the trench shape which affects the

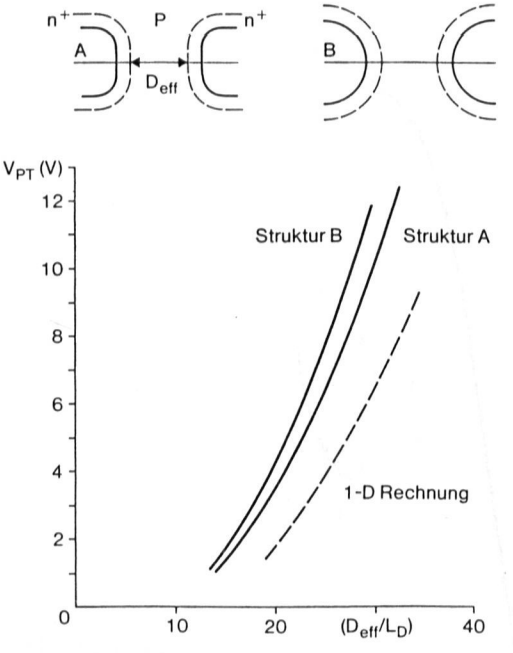

Fig. 3: Punch through voltage as a function of the normalized trench to trench distance for different trench geometries, as indicated in the insert.

field distribution between the neighbouring trenches. The electron density for an applied voltage of V_{tt} = 6 V is shown in Fig. 4. For homogeneously doped substrate punch through takes place between the Si surface and a depth of 4.5 µm.

To minimize the cell size of a 4 Megabit DRAM the influence of the trench depth and three different p-well profiles, shown in Fig. 5, on the leakage behaviour has been studied. The shape of the trenches was taken from REM photographs and approximated by the parameters in Fig. 1. The trenches have a cylindrical cross section with 1.1 µm in diameter. The depth was varied between 5.0 and 6.0 µm. The HiC doping profile was determined by SIMS measurements. For simplicity all doping profiles are approximated by exponential functions. The manual grid was designed to get a good resolution of the geometry, the doping profiles and the leakage channel in punch through conditions. It was found that a maximum number of 40 000 grid points is enough for accurate and stable results. The analytical punch through model

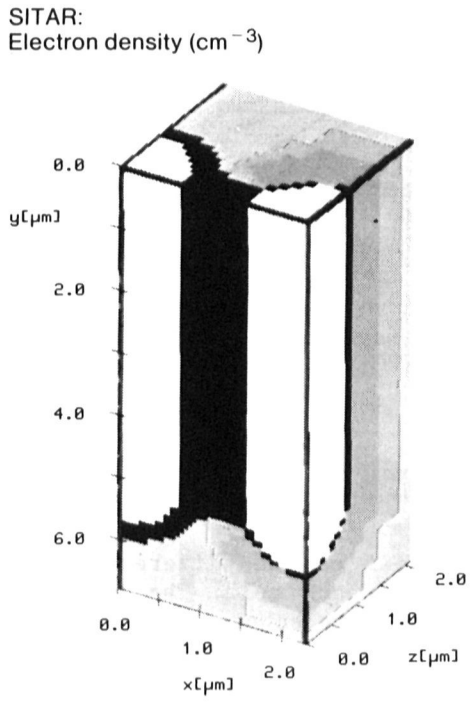

Fig. 4: Electron density distribution at V_{tt} = 6 V for homogeneously doped substrate (2E16cm^{-3}).

described in the last section was used to get a initial guess for the punch through voltage V_{pt}. Therefore the I-V characteristic in the interesting region could be calculated by only 3 - 4 selected voltages. From the leakage currents the punch through voltage has been extracted by assuming a critical current of 1pA. The punch through voltage V_{pt} as a function of the trench to trench distance is shown in Fig. 6 for the trench depths 5.0, 5.5 and 6.0 μm, and for the p-well types labelled by I, II and III in Fig. 5. The punch through curves become steeper with increasing doping density. Assuming a maximum trench depth of 5.5 μm, the well types I and II can be used for trench to trench distances down to D = 1.2 μm, whereas type III allows only 1.3 μm. However, due to technological variations the nominal distance should be increased by about 0.2 μm.

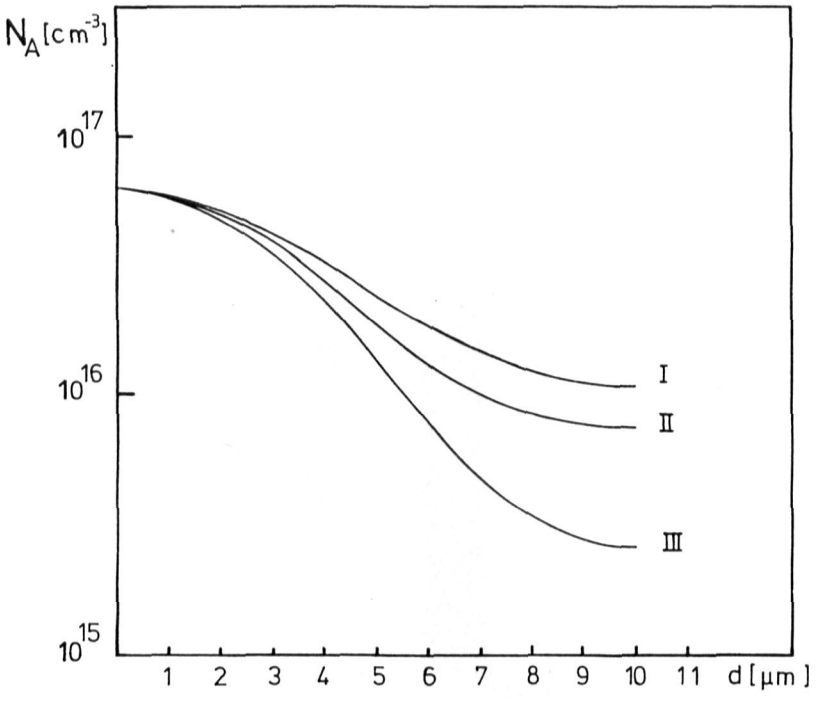

Fig. 5: Doping profile of the different p-wells used in the optimization of the trench cell. The concentration at large depths is identical to the substrate doping.

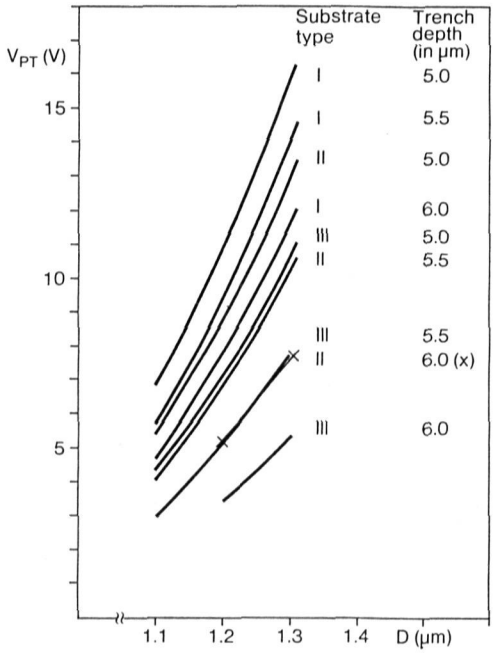

Fig. 6: Punch through voltage as a function of trench to trench distance for various p-well profiles and trench depths.

The leakage path can be detected by analyzing the electron density distribution around the trench capacitors for $V_{tt} < V_{pt}$. Fig. 7 shows the electron distribution for the well type II, the trench depth 5.5 /um and the distance D = 1.2 /um at V_{tt} = 6 V, just before the critical leakage current is reached. The leakage path is in a depth of 4 /um. In this region the ratio of effective trench-trench distance to Debye length has a maximum. Between the surface and the critical depth the doping concentration and for large depths the shape of the trench bottom inhibit punch through.

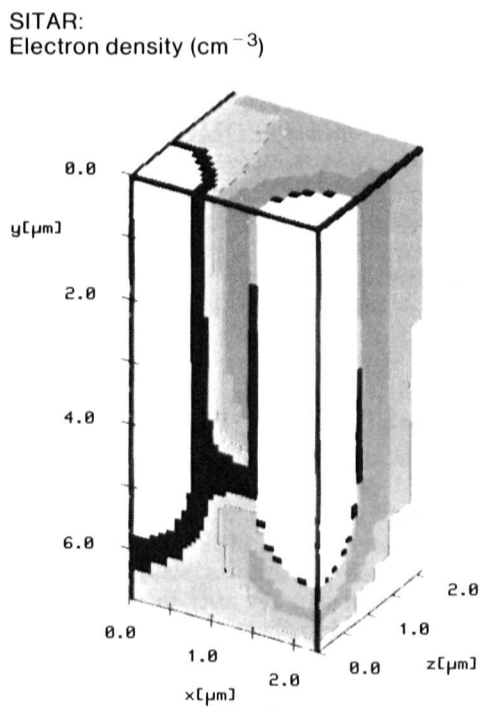

Fig. 7: Electron density distribution between two neighbouring trench capacitors for V_{tt} = 6 V, the well type II and the geometry parameters T_1 = 5.5 /um, R_1 = 0.55 /um, R_2 = 0.4 /um and trench to trench distance D = 1.2 /um.

CONCLUSIONS

The 3-dimensional device simulator SITAR has been introduced which allows the analysis of trench type structures. It solves the classical semiconductor equations on a finite difference mesh by using Gummel's method and a very efficient solution algorithm for the linearized equations. The simulator has been used to investigate punch through between neighbouring trench capacitors depending on geometry and doping profiles, and to optimize the cell size for 4 Megabit DRAMs. The different punch through behaviour of trench capacitors in p-wells and those in homogeneously doped substrate results from a compression of the leakage channel by the 3-dimensional field distribution.

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