AN INVESTIGATION OF THE EFFECTS OF RECESSED-GATE GEOMETRY ON MESFET PERFORMANCE

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SUMMARY

This paper presents the preliminary results of an investigation of the effect of the recess geometry on the breakdown characteristics of a GaAs MESFET. It is found that the angle of the recess may affect the the gate-drain breakdown voltage of the device, shallower angles performing better than sharper angles. Placing the gate contact towards the source end of the recess has also been found to improve the breakdown performance.

1 INTRODUCTION

The output power of a GaAs MESFET is determined by the maximum voltage swing that it can sustain and the maximum current that it can pass. The current is limited by velocity saturation of carriers in the channel. Although increasing the device channel width can directly enhance the output current, it may give rise to difficulties in matching the input impedance. Consequently, attempts to improve the power handling capability of GaAs MESFETs have concentrated on maximizing the voltage swing. However, an important factor that limits the maximum voltage swing is avalanche breakdown between the gate and the drain.

The use of a recessed-gate geometry has been found experimentally to give rise to a marked improvement in the device power handling capability [1]. The results of experimental studies of impact ionization of such devices [2] also indicate that in planar structures, breakdown begins under the drain, whereas in recessed devices breakdown begins under the gate at a higher value of drain-source voltage. Electrical breakdown of the device is also strongly affected by the surface [3]. This is due to the high density of surface states, which give rise to surface depletion and a very high recombination velocity, thus quenching avalanche breakdown in the vicinity of the surface.

Various recess geometries are used in practical MESFETs, but to date little work [4,5] has been done to investigate the effect of these geometries on the device breakdown. In this paper, we present the preliminary results of an investigation of the effect of the recess geometry on the breakdown behaviour of a MESFET.

2 METHOD OF SIMULATION

The basic transport equations describing the dynamics of particles within a GaAs MESFET are solved two-dimensionally subject to appropriate initial and boundary conditions. The finite element device simulator SEDSIM [8], developed at the University of Birmingham, is used to perform the above task. SEDSIM is flexible in handling complicated geometries and boundary conditions, and is easy to use due to its sophisticated preprocessor and postprocessor facilities. An implicit time scheme with efficient solution algorithms is employed. Various generation and recombination processes have been included. An additional option available in the simulator is the dynamic treatment of impact ionization using a sophisticated two-dimensional model, instead of the static one-dimensional model commonly used in the literature.

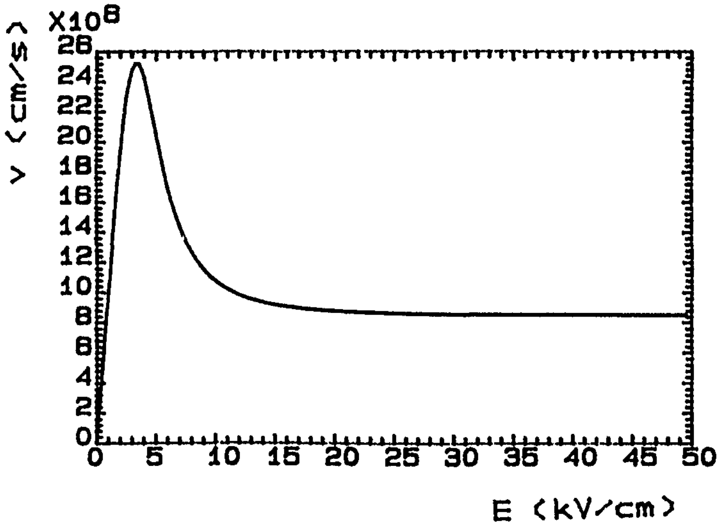
The use of accurate models of mobility and diffusion coefficient in the transport equations is important, since the negative differential resistance of GaAs gives rise to formation of a strong dipolar domain, the dynamics of which are strongly dependent on the exact values of mobility and diffusion coefficient used. The diffusion coefficient and mobility vs. E-field used are shown in fig. 1. These are based on experimental data given in [6] and Monte Carlo data given in [7].

3 EFFECT OF RECESS ANGLE

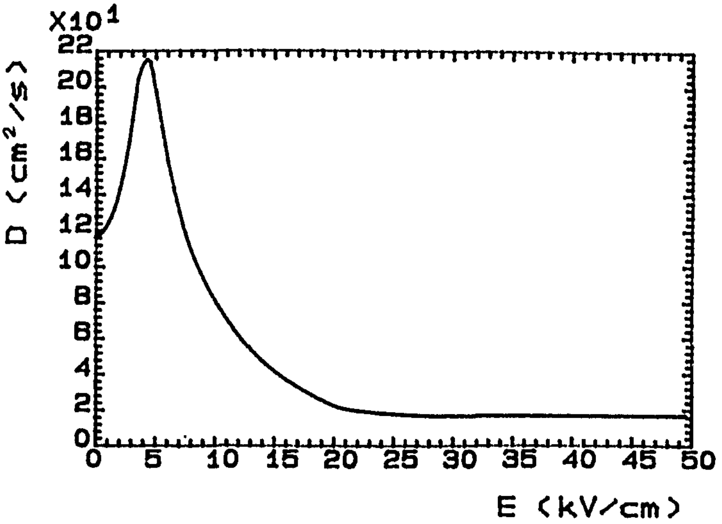
To investigate how recess angle affects the device performance, the four basic structures shown in figs. 2a-2d were used. These are :

(a) a planar structure
(b) a rectangular recess
(c) an obtuse angled recess
(d) an acute angled recess

The active layer is n-type GaAs of thickness 0.2 µm and doping density 10^{15} cm^{-3} . The gate-drain spacing and the recess depth are kept constant at 1.2 µm and 0.2 µm respectively. The substrate is assumed to be undoped.

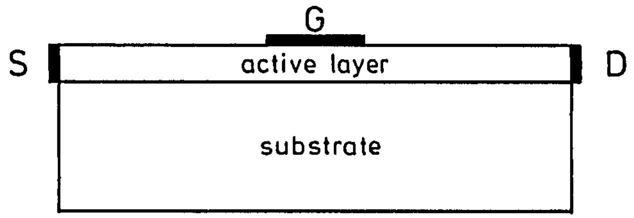


(a) velocity versus electric field

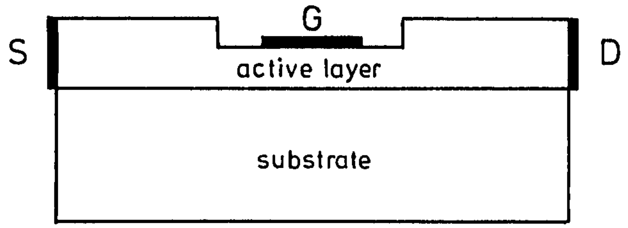


(b) diffusion coefficient versus electric field

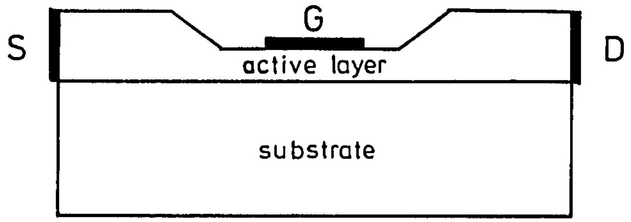
Fig. 1 Variation of velocity and diffusion coefficient with electric field for GaAs



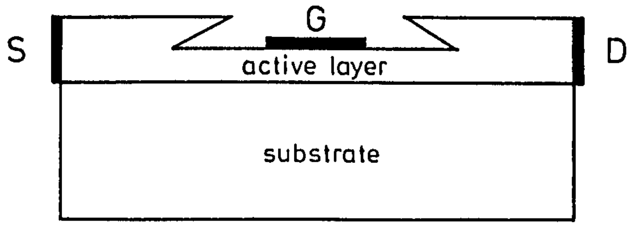
(a) planar structure



(b) rectangular recess



(c) obtuse angled recess



(d) acute angled recess

Fig. 2 Planar and recessed gate structures modelled

The four structures were simulated for Vgs = -1V and Vds varying from 8V to 30V. The current-voltage characteristics of the four structures are shown in fig. 3. The planar device has a lower value of the source-drain saturation current than the recessed-gate devices because of its higher parasitic source and drain resistance. The acute-angled recess device is the first of the recessed structures to break down and the last is the obtuse-angled recess structure. The planar structure breaks down first, as expected. The difference in breakdown voltage between the planar and recessed structures is fairly small. This is perhaps because of the relatively low values of source-drain current caused by the low doping and narrow active layer. As will be seen in the following, the breakdown of the planar device is affected by the drain-source current to a greater extent than are the recessed-gate structures.

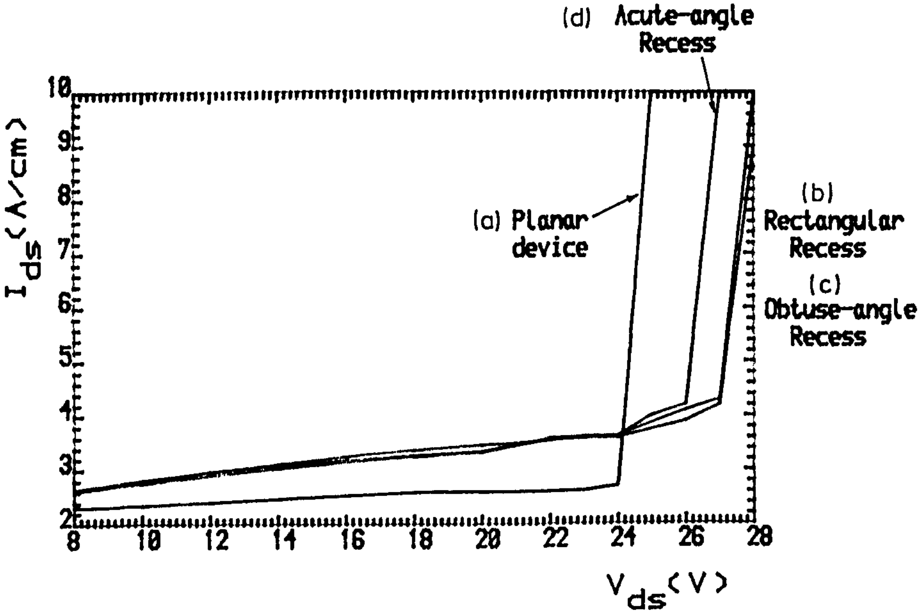


Fig. 3 Current voltage characteristics of the four MESFET structures shown in fig. 2a-2d

Figs. 4a and 4b present the potential distribution in the planar and the obtuse-angled recess structures for Vgs = -1V and Vds = 18V. At this bias condition, neither of the devices has broken down. It can be seen that the effect of the recess is to reduce the electric field in the vicinity of the drain and to give rise to a corresponding increase in electric field near the gate. This is because of the larger amount of space charge that exists in a recessed-gate structure for a given drain bias.

Figs. 5a and 5b show the impact ionization in these structures for Vds=18V. The corresponding result for Vds=10V is given for the planar device in fig. 6. In the recessed-gate structure, the impact ionization is concentrated at the drain end of the gate for both high and low values of drain bias. However, in the planar structure, as can be seen by comparing fig. 5a and fig. 6, there is a switchover from weak ionization at the drain end of the gate for low drain voltages to strong ionization at the drain edge for high voltages.

It is instructive to examine the total ionization rate in the devices as a function of drain voltage as shown in fig. 7. For the recessed-gate structures, the total ionization rates increase steadily as the drain voltage is increased. Ionization in structures (b) and (d) is stronger than in structure (c), the acute angled recess showing the strongest ionization. The planar device has a much smaller ionization rate at low drain voltages, but for Vds between 12V and 16V, the rate rises to a value comparable to that of the recessed-gate devices. This corresponds to the transition from the behaviour of fig. 6 to that of fig.5a, where in the first case the ionization is predominantly at the drain end of the gate, whereas in the second case it occurs predominantly in the region of high current density at the drain edge. It is to be noted that the planar device breaks down in a region of high current density and relatively low electric field, whereas the recessed-gate device breaks down in a region of low current density and high electric field. This confirms the previously mentioned observation that the breakdown voltage of the planar device depends strongly on the source-drain current, but the breakdown voltage of the recessed-gate device does not.

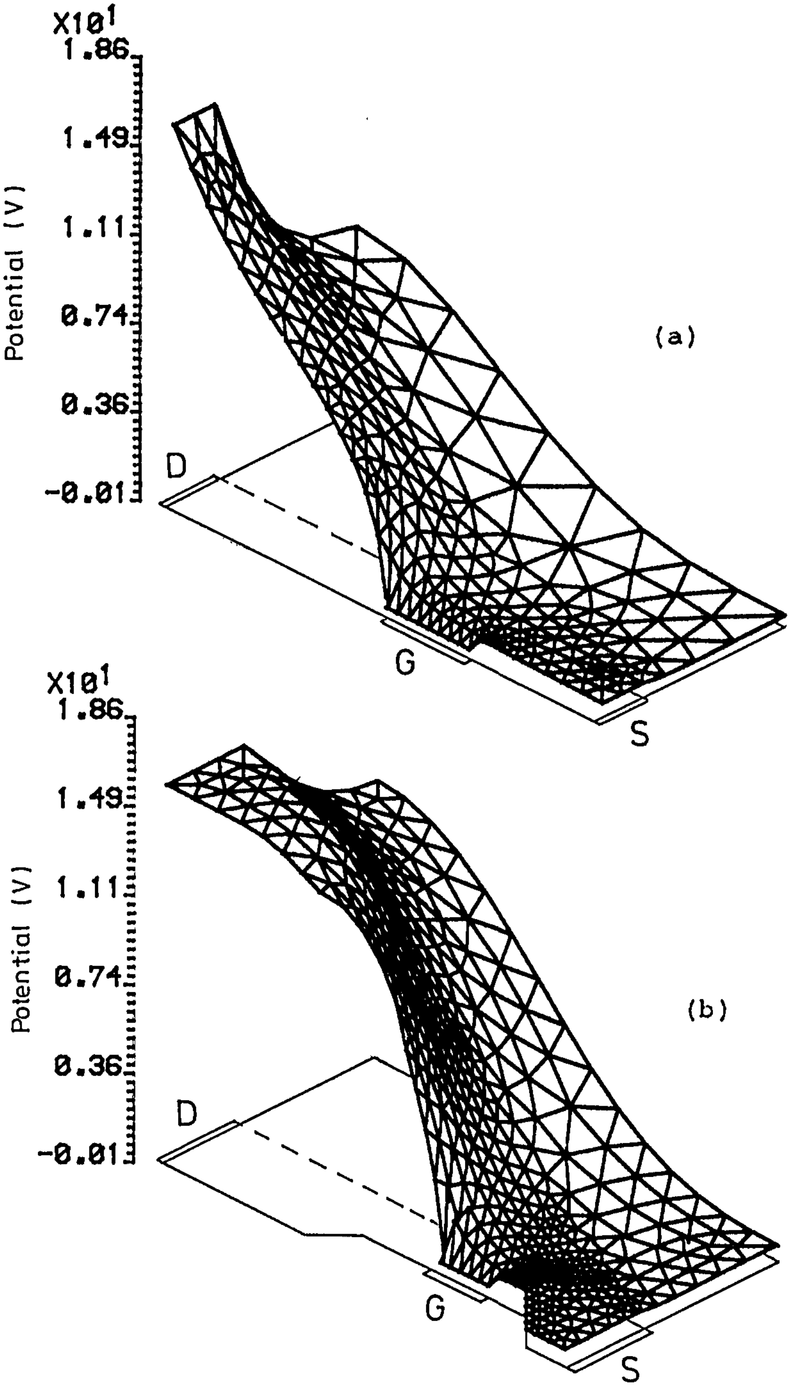


Fig. 4 Potential distribution in
(a) the planar device
(b) the device with the obtuse-angled recess
Vgs=-1V, Vds=18V

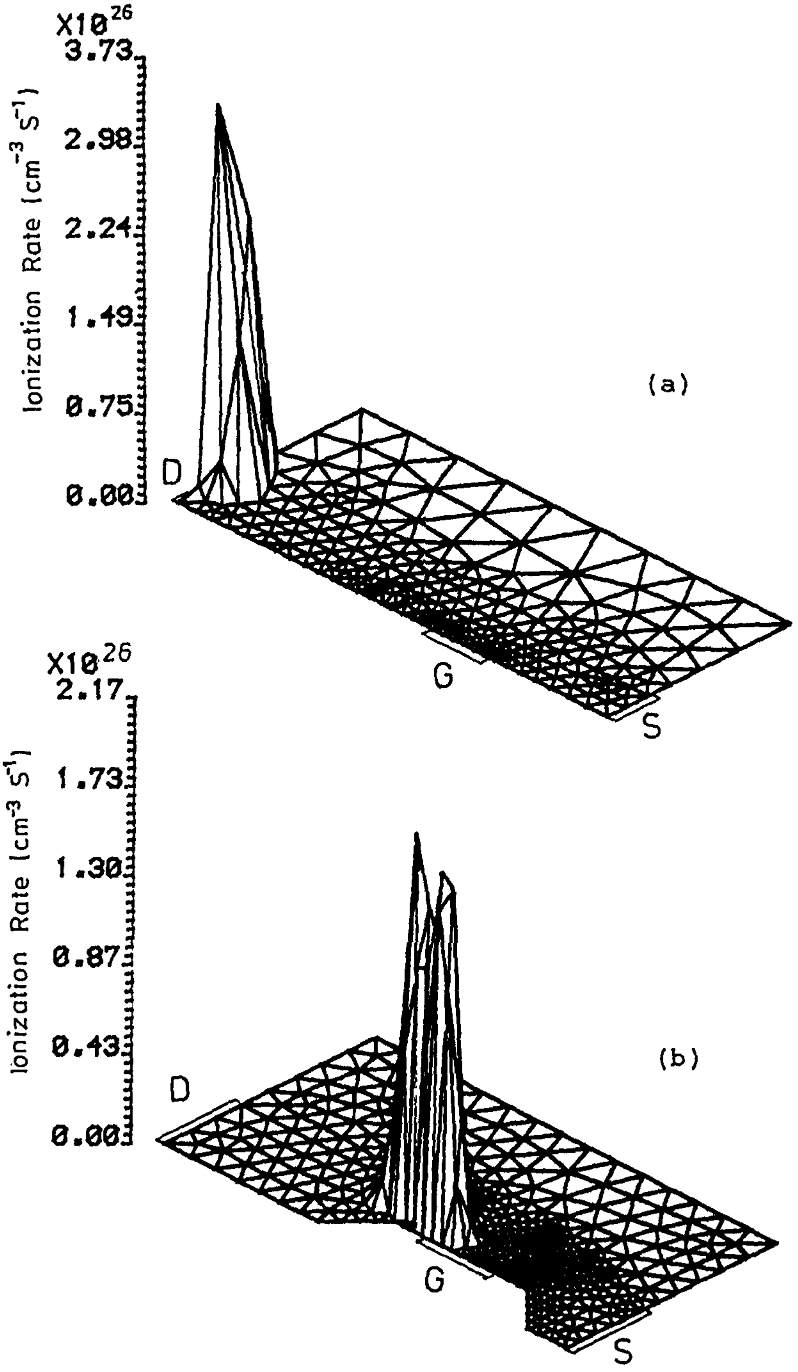


Fig. 5 Impact ionization in
(a) the planar device
(b) the device with the obtuse-angled recess
Vgs=-1V, Vds=18V

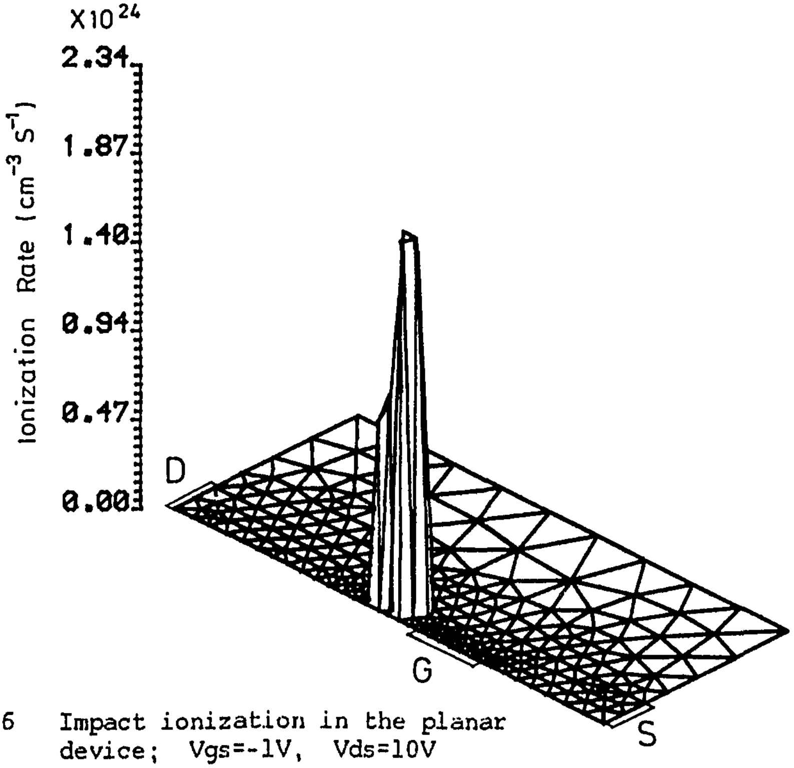


Fig. 6 Impact ionization in the planar device; Vgs=-1V, Vds=10V

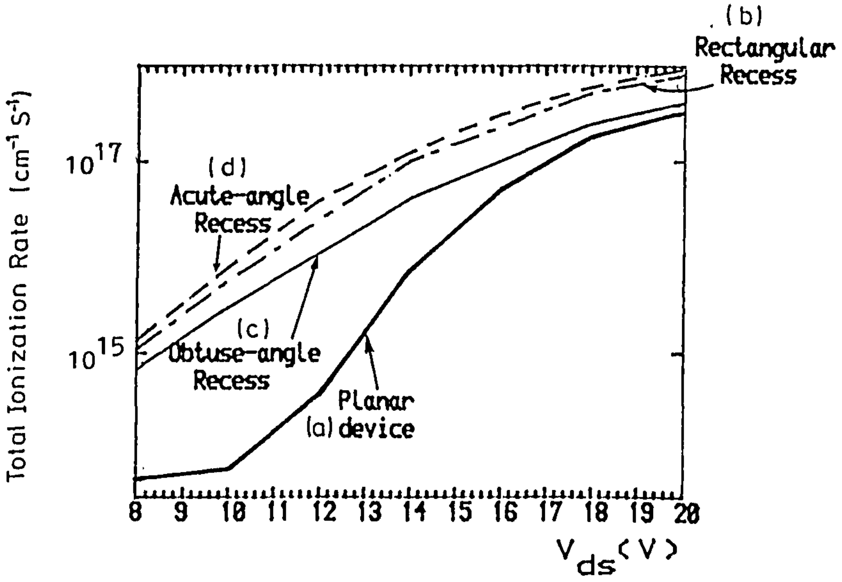


Fig. 7 Total ionization rate in the MESFET devices shown in fig. 2a-2d as a function of drain voltage

4 EFFECT OF GATE POSITION

The effect of the gate position within the recess was investigated by examining the three devices shown in fig. 8. The structure in fig. 8b is identical to that in fig. 2b, the gate being symmetrically placed in the centre of the recess. In fig. 8a and 8c the gate is displaced 0.1 µm closer to the source and 0.1 µm closer to the drain respectively.

Fig. 9 presents the current-voltage characteristic of the three devices. It can be seen that the further the gate is from the drain end of the recess, the higher the breakdown voltage. Fig. 10 shows the variation of the total ionization rate for the three structures against the drain-source voltage. This shows that the structure with the gate displaced toward the source has consistently less impact ionization than the basic structure of fig. 8b by about a factor of three, and the structure with the gate displaced toward the drain has a consistently higher impact ionization than the basic structure by almost a factor of two.

The reason for this behaviour can be seen from fig. 11, where the potential distributions of the three devices are plotted for Vgs=-1V and Vds=18V. The recess edge pins down the edge of the depletion layer with the result that almost the same voltage is to be dropped across the recess in all three cases. Consequently, the smaller the distance is between the gate and the recess edge, the lower the electric field is in the recess region and hence the lower the breakdown voltage.

5 CONCLUSIONS

Various MESFET structures were simulated, with varying angle of recess and varying gate position within the recess. It was found that the angle of recess has an appreciable effect on the breakdown voltage of the device, shallower angles performing better than sharper angles. It was also found that the breakdown voltage of the device is improved by moving the gate contact toward the source end of the recess.

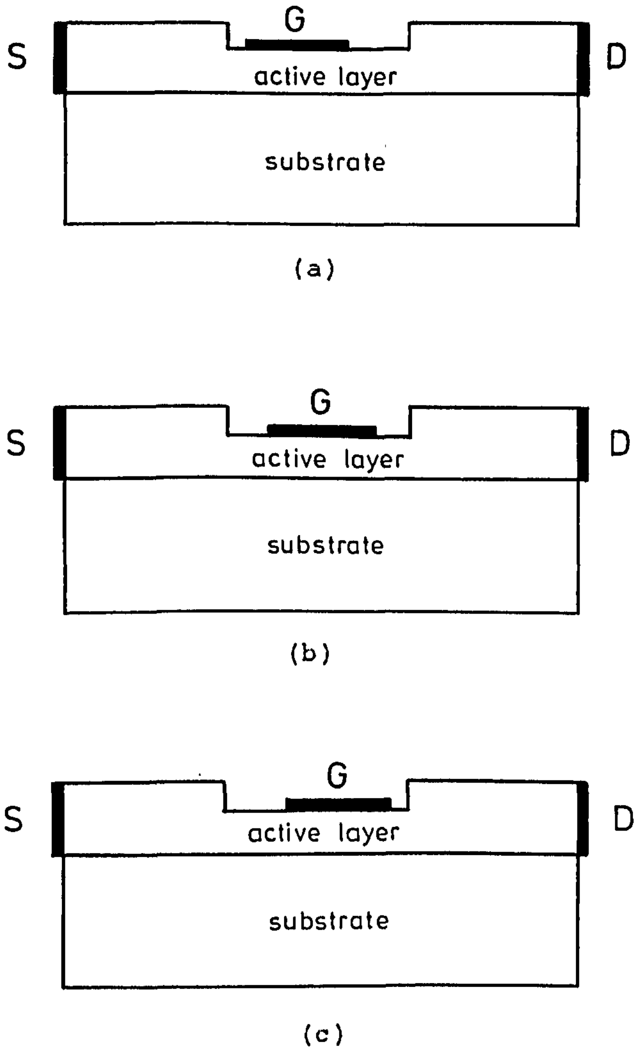


Fig. 8 Recessed structure with the gate contact position:
(a) near the source edge of the recess
(b) in the centre of the recess
(c) near the drain edge of the recess

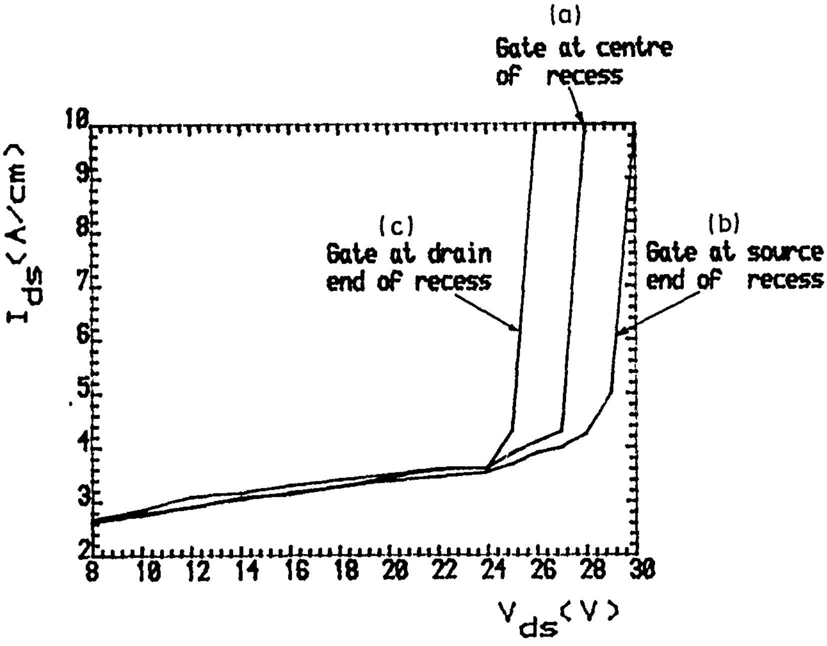


Fig. 9 Current-voltage characteristic of the three MESFET devices shown in fig. 8a-8c

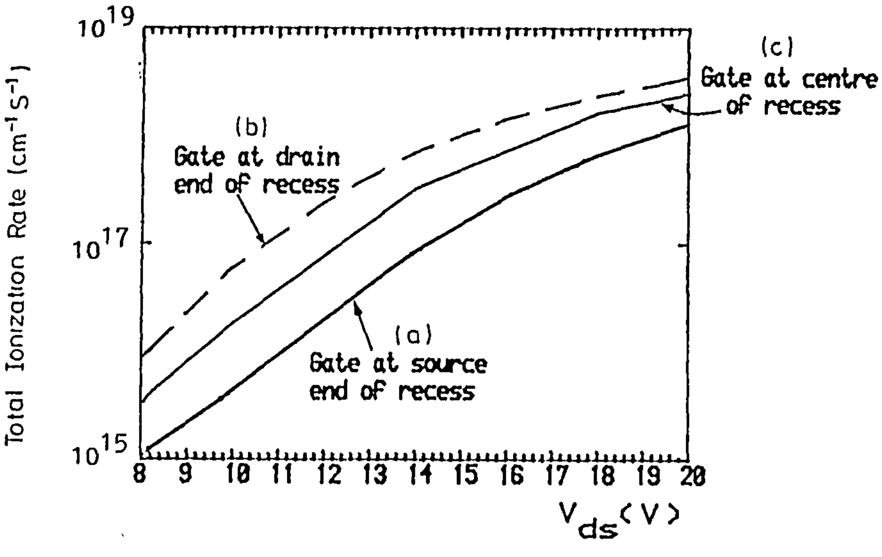


Fig. 10 Total ionization rate in the structures shown in fig. 8a-8c as a function of drain voltage

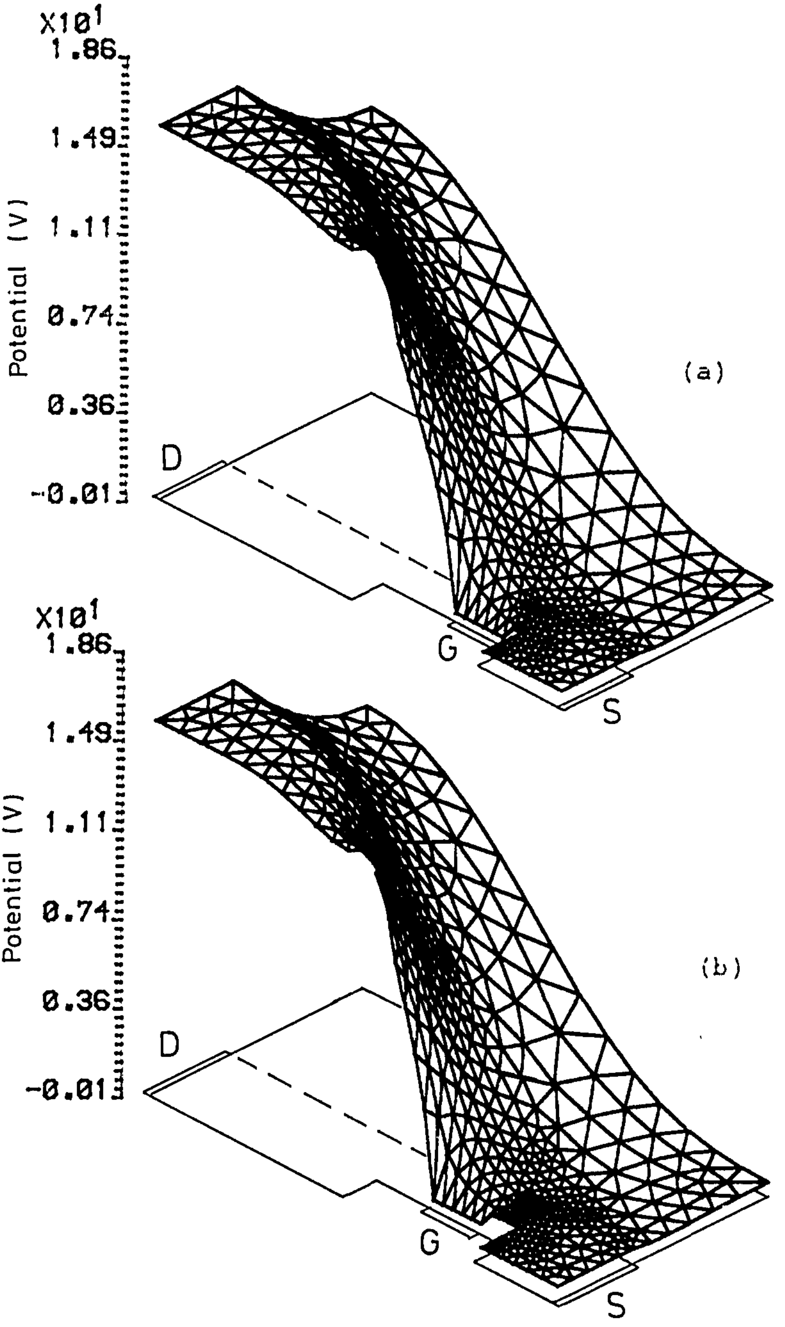


Fig. 11 Potential distibution in the devices shown in fig. 8a-c
(a) gate near the source edge of the recess
(b) gate in the centre of the recess
(c) gate near the drain edge of the recess
Vgs=-1V, Vds=18V

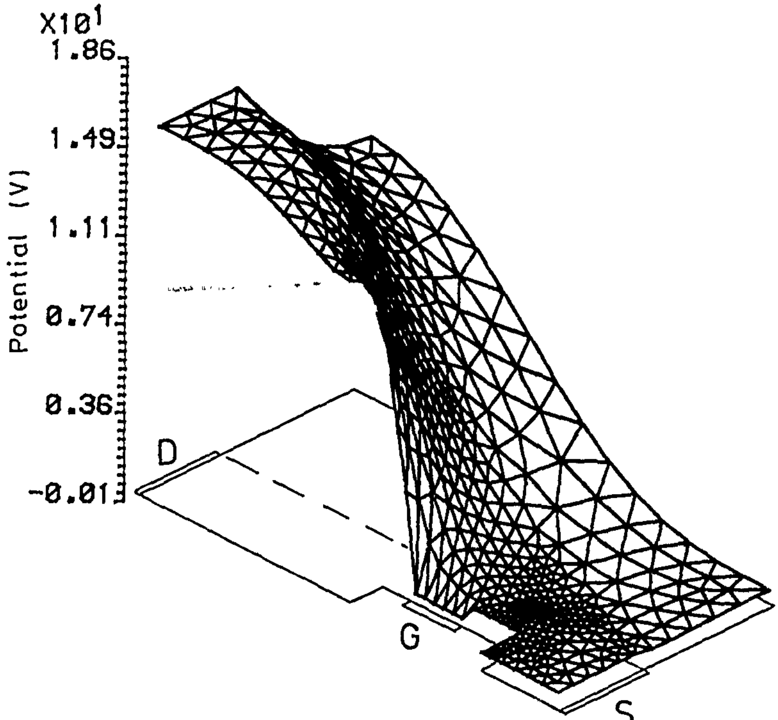


Fig. 11 (c)

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