

A PHYSICAL PARAMETRIC DEVICE MODEL FOR CMOS CIRCUIT SIMULATION

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SUMMARY

A new single expression MOSFET model suitable for simulation of analog and digital CMOS circuits is presented, including a new rigorous treatment of accumulation (majority carrier, normally off) devices.

Doping and resistance parameters are obtained directly from processing simulation and layout programs. Mobility and small geometry effects are included. The model has been verified using fourteen n- and p-type devices.

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A MOSFET model has been derived for accurate CMOS circuit simulation which represents a compromise between an empirical table-lookup model and a physical but time-consuming 2- or 3-D model. The model described here advances the state of the art by incorporating the following features:

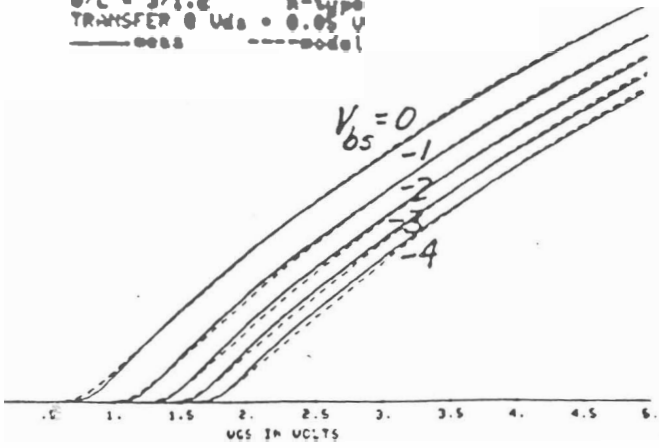
- (1) Single expression inversion and accumulation models are formulated in voltage space, making the models suitable for analog and digital CMOS circuit simulation at current levels from subthreshold to saturation.
- (2) A more rigorous accumulation model (majority carrier, normally off), derived from a generalized field function common to both types of CMOS device, supercedes the previously described model [1].
- (3) The implanted doping profile, as obtained from a process simulation program such as SUPREM-3, is used directly to give the body effect.
- (4) Source and drain resistances are used directly as obtained from layout.
- (5) Drain-induced barrier-lowering is expressed in a new form involving the derivative of surface potential with respect to gate voltage.
- (6) All important small geometry effects are included in parametric form, including a new expression for channel-length modulation which reflects the competition for charge between the drain and gate voltages.
- (7) Parameters for mobility degradation due to parallel and perpendicular fields, including variation of high field parameters with channel length, are included in the model.

A key step is to formulate the model in voltage space rather than configuration space. This allows dependent variables such as charge and current to be expressed in terms of the three applied voltages: gate, drain, and substrate. In this form the model can readily be implemented in a circuit simulation program, e.g. SPICE. Furthermore, because charge is computed as a preliminary step, the model is also suited to the calculation of capacitance, although this task is not yet complete.

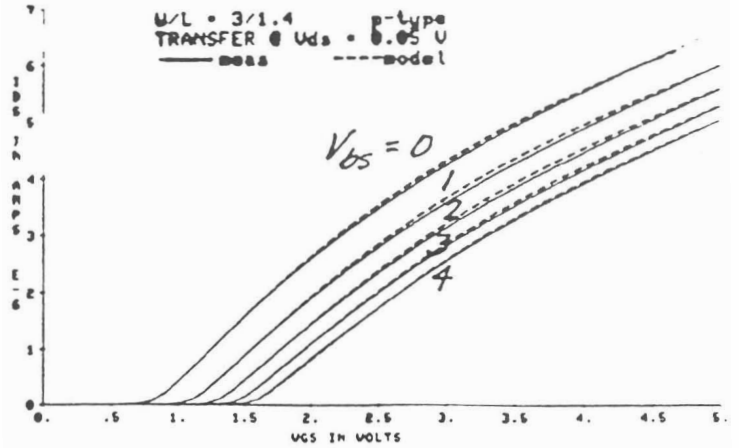
The model has been verified by its application to fourteen n- and p-type devices whose channel width-to-length ratios W/L vary from 100/100 to 3/1.2 microns/microns. The measured and computed transfer and drain characteristics given in the accompanying figures show good agreement. Because the new model has a firmer physical basis than its predecessors, and includes the doping profile and series resistance in a physically meaningful way, the variation of the two high field mobility parameters with channel length can be described within the model in terms of simple functions.

A companion paper gives details of the implementation of the new model in the SPICE circuit simulation program. The results of application of the model to a variety of analog and digital circuits is also given.

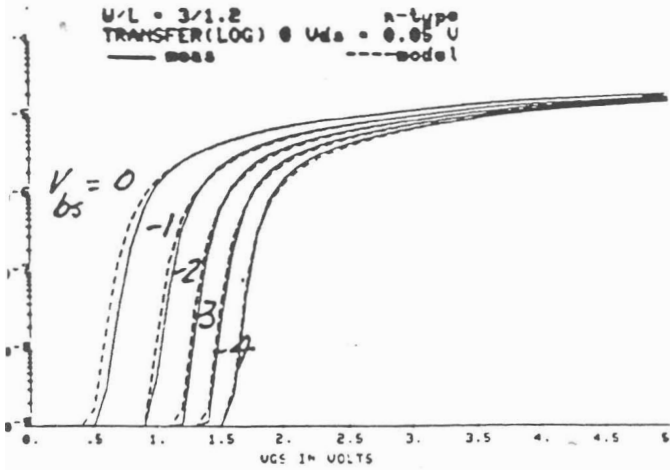
U/L = 3/1.2 n-type
TRANSFER @ U_{ds} = 0.05 U
— meas --- model



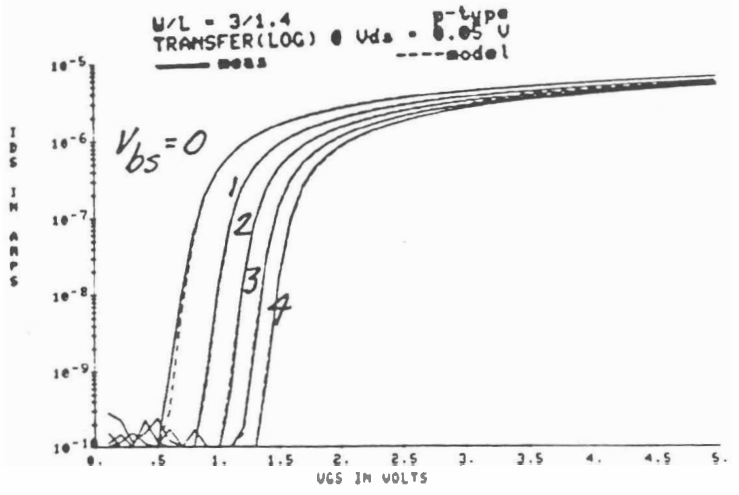
U/L = 3/1.4 p-type
TRANSFER @ U_{ds} = 0.05 U
— meas --- model



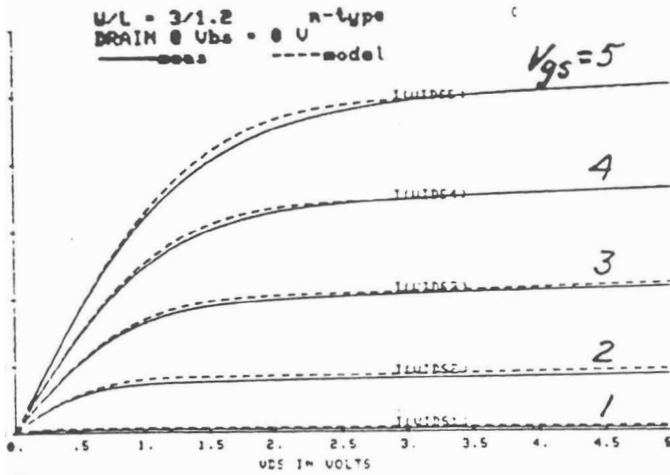
U/L = 3/1.2 n-type
TRANSFER (LOG) @ U_{ds} = 0.05 U
— meas --- model



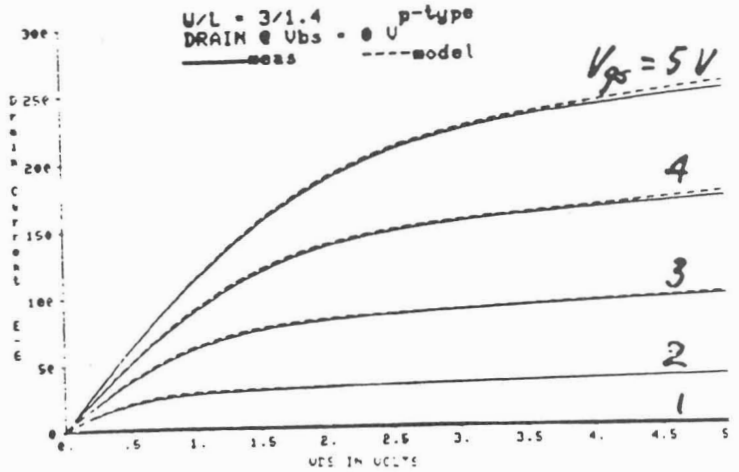
U/L = 3/1.4 p-type
TRANSFER (LOG) @ U_{ds} = 0.05 U
— meas --- model



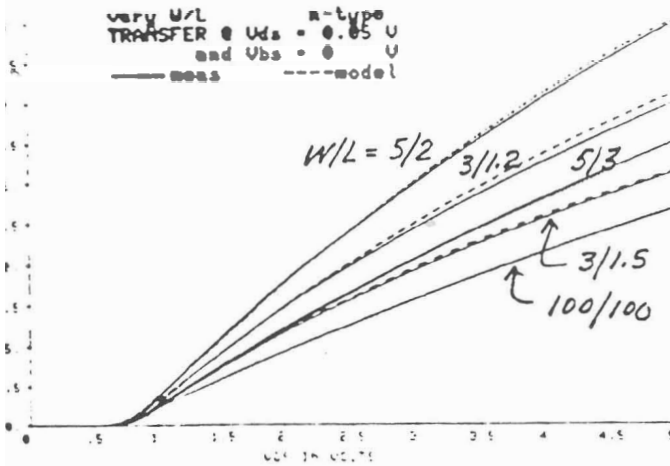
U/L = 3/1.2 n-type
DRAIN @ U_{bs} = 0 U
— meas --- model



U/L = 3/1.4 p-type
DRAIN @ U_{bs} = 0 U
— meas --- model



vary U/L n-type
TRANSFER @ U_{ds} = 0.05 U
and U_{bs} = 0 U
— meas --- model



vary U/L p-type
TRANSFER @ U_{ds} = 0.05 U
and U_{bs} = 0 U
— meas --- model

