A Circuit Simulation Model for Bipolar Induced Breakdown in MOSFET

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SUMMARY

A bipolar-induced breakdown model for MOSFET was developed for circuit simulation. The model was successfully applied to model short-channel transistor breakdown characteristics with effective channel length down to 0.6 micron; the sudden increase in the MOS drain current due to threshold voltage reduction due to the forward biasing of the source-substrate junction is also modeled with considerable accuracy. To our knowledge, this is the first successfull application of short-channel breakdown model in a circuit simulator [1]. Model parameter extraction and installation of the model in the circuit simulator will also be discussed.

ABSTRACT

I. THE BIPOLAR-INDUCED BREAKDOWN MODEL

The physically based bipolar-induced breakdown model of Hsu et al [2] was extended and parameterized. The simple parametric substrate current impact ionization model developed by Mar [3] et al was used instead of the one described in [2] which requires numerical integration. A simple channel length dependence was added to the gain of the lateral parasitic bipolar transistor to allow the model to account for MOSFET I-V characteristics at various channel lengths. The physics of the model is summarized in Fig.1.

II. PARAMETER EXTRACTION.

The model has four parameters α_o and L_o model the common base current gain of the lateral parasitic bipolar and its channel length dependence, respectively; ϵ is a parameter that accounts for the fact that electrons which flow deeper in the substrate experience less electric field than channel electrons, and R_{sub} models the substrate spreading resistance.

The model parameters were extracted in the following sequence of steps. In each step, a modified Marquardt-Levenberg parameter optimizer was used to extract the parameters, using measured data from several device geometries. First, the geometrical parameters, and zero field long-channel mobility parameters are extracted, followed by the threshold voltage related parameters extraction, and then all the low drain voltage I-V related parameters are extracted (using only data points below breakdown). In the next step, the impact ionization related parameters [3] were obtained, using only substrate current data for drain voltages below the parasitic bipolar turn-on). Finally, the I-V measured data, including the high V_{DS} were used to extract the bipolar induced breakdown model parameters.

The result for an N channel transistor with effective channel length of 0.6 micron is shown in Fig.2; note that good fit to measured transistor data is obtained, both in the breakdown region and in the region of onset of parasitic bipolar turn-on; the sudden increase (the kink at V_{DS} = 4V) in the MOS drain current due to threshold voltage reduction due to the forward biasing of the source-substrate junction is also modeled with considerable accuracy. The kinks are more pronounced at high substrate bias, and occur at lower drain voltages for higher values of substrate resistance.

The comparison for a short-channel transistor at high voltage is shown in Fig. 3.

III. CIRCUIT SIMULATION RESULTS

The model was installed in ISPEC (Intel Simulation Program for Electronic Circuits). In this talk we will also discuss the installation of the model in the circuit simulation program as well as the simulation results in analog and digital circuits.

This model could be used to predict the device lifetime and reliability (due to hot-electron induced threshold shifts and mobility degradation).

REFERENCES

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[2] F.C. Hsu, P.K.Ko, S.Tam, C.Hu and R.S.Muller, IEEE Trans. ED-29, p.1735, 1982.
[3] J.Mar, S.S.Li and S.Y.Yu, IEEE Trans. CAD-1, p.183, 1982.

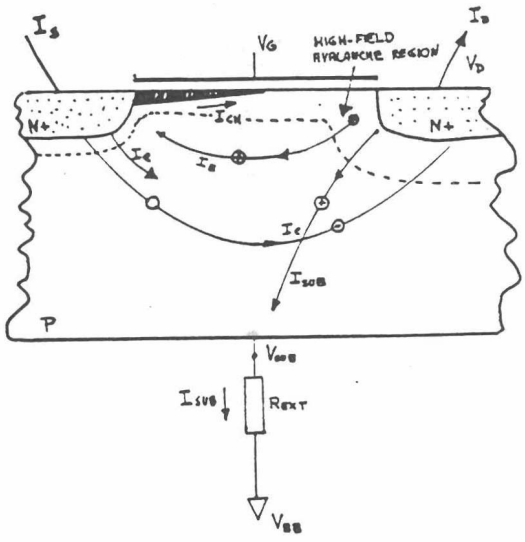

Figure 1

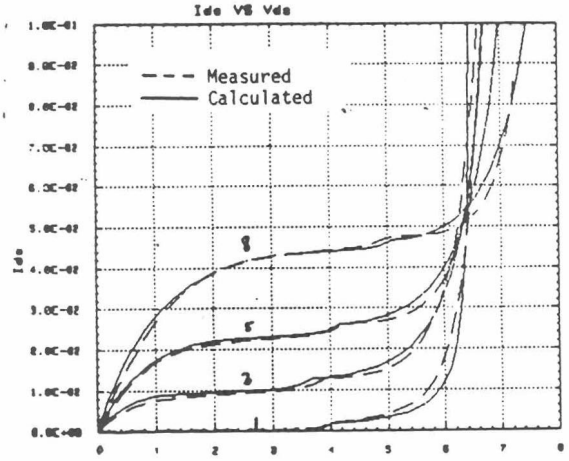

Figure 2

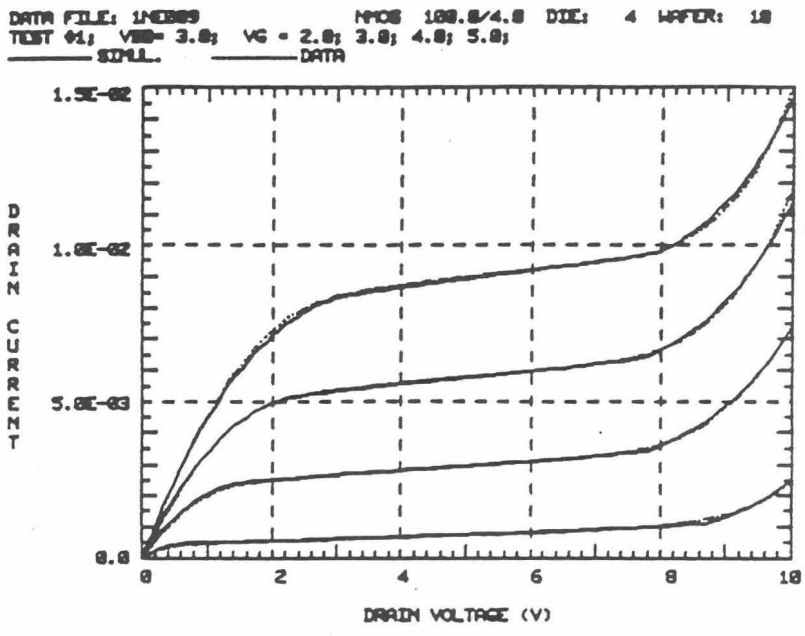

Figure 3